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| Document No. | | Issue date | 2016/01/07 | Revision | 02 |

# Customer Approval Specification

**Customer：** 苏州与来视讯科技有限公司

**Product Name: M080AWT8 R1**

**Document Issue Date: 2016/01/07**

| Customer | InfoVision Optoelectronics |
|---|---|
| **SIGNATURE**<br><br>Please return 1 copy for your confirmation with your signature and comments. | **SIGNATURE**<br><br>**REVIEWED BY CQM**<br><br>**PREPARED BY FAE** |

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2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by IVO for any intellectual property claims or other problems that may result from application based on the module described herein.

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## 1.0 General Descriptions

### 1.1 Introduction

The M080AWT8 R1 is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel, a driver circuit and a backlight system. This TFT LCD has a 8.0 inch diagonally measured active display area with WSVGA resolution (1,024 horizontal by 600 vertical pixels array).

### 1.2 Features

- Supported WSVGA Resolution
- LVDS Interface
- Compatible with RoHS Standard

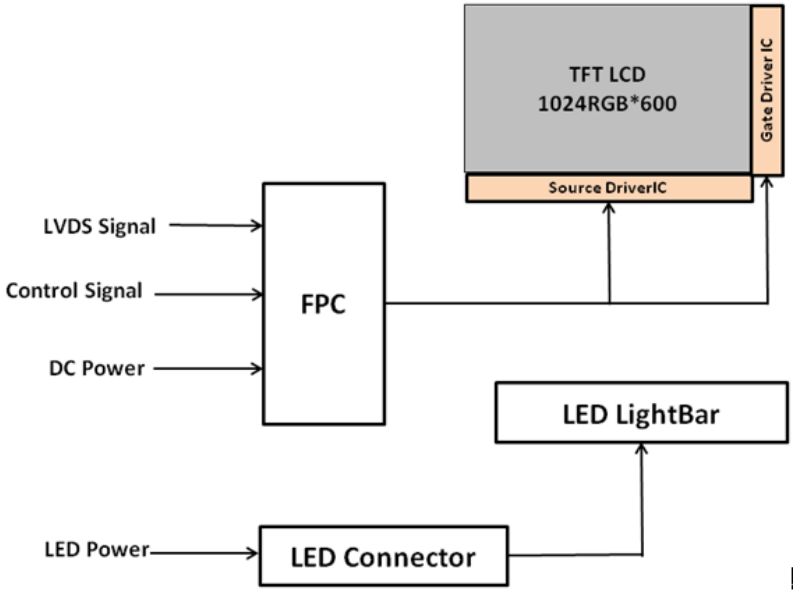
### 1.3 Product Summary

| Items | Specifications | Unit |
|---|---|---|
| Screen Diagonal | 8.0 | inch |
| Active Area (H x V) | 176.64 x 99.36 | mm |
| Number of Pixels (H x V) | 1,024 x 600 | - |
| Pixel Pitch (H x V) | 0.1725 x 0.1656 | mm |
| Pixel Arrangement | R.G.B. Vertical Stripe | - |
| Display Mode | Normally White | - |
| White Luminance ☆ | 670(Typ.) | cd /m$^2$ |
| Contrast Ratio ☆ | 800 (Typ.) | - |
| Response Time | 16 (Typ.) 25(Max) | ms |
| Input Voltage | 3.3 (Typ.) | V |
| Power Consumption | 4.6 (Max.) | W |
| Weight | 240 (Max.) | g |
| Outline Dimension (H x V x D) | 192.8(Typ.) x 116.9(Typ.) x6.4 (Typ.) | mm |
| Electrical Interface (Logic) | LVDS | - |
| Support Color | 16.7M | - |
| NTSC | 72 (Typ.) | % |
| Viewing Direction | 6 O'clock | - |
| Surface Treatment | Anti-glare | - |

### 1.4 Functional Block Diagram

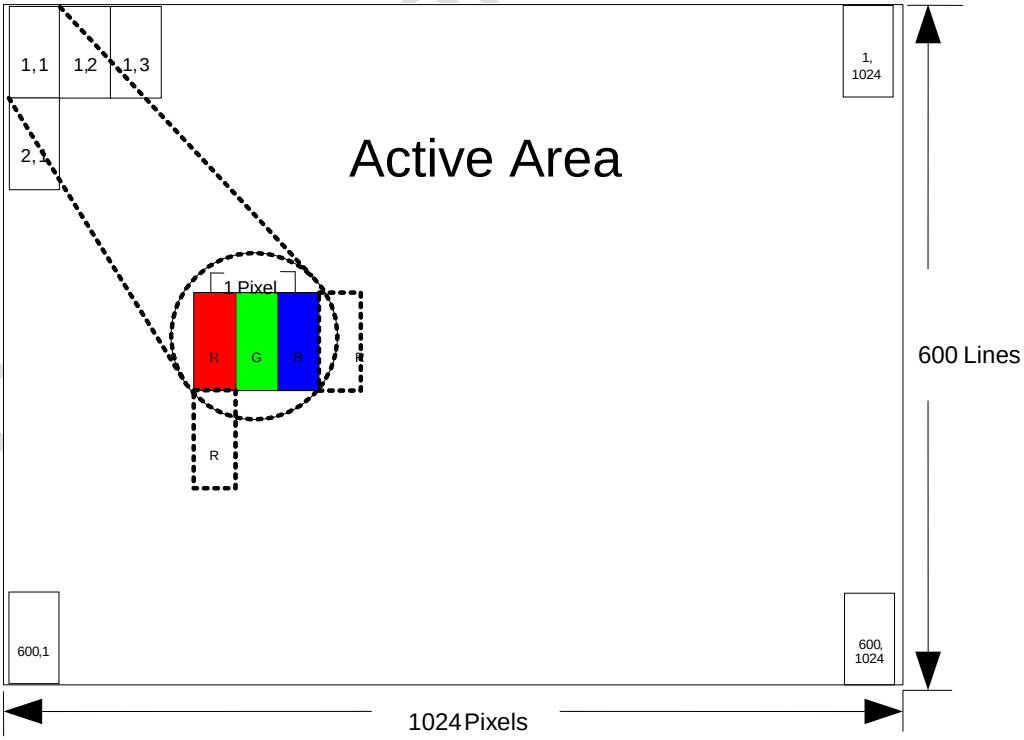
Figure 1 shows the functional block diagram of the LCD module.

**Figure 1 Block Diagram**




### 1.5 Pixel Mapping

**Figure2 Pixel Mapping**



## 2.0 Absolute Maximum Ratings

**Table 1 Electrical & Environment Absolute Rating**

| Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Digital Supply Voltage | $V_{DD}$ | -0.5 | - | 3.9 | V | (1),(2) |
| Logic Input Signal Voltage | $V_{Signal}$ | -0.5 | - | 3.9 | V | |
| Operating Temperature | $T_{OP}$ | -30 | - | 85 | ℃ | (3),(4),(5),(6) |
| Storage Temperature | $T_{ST}$ | -40 | - | 90 | ℃ | |

Note (1) Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under normal operating conditions.

Note (2) Operating temperature 25℃, humidity 55%RH.

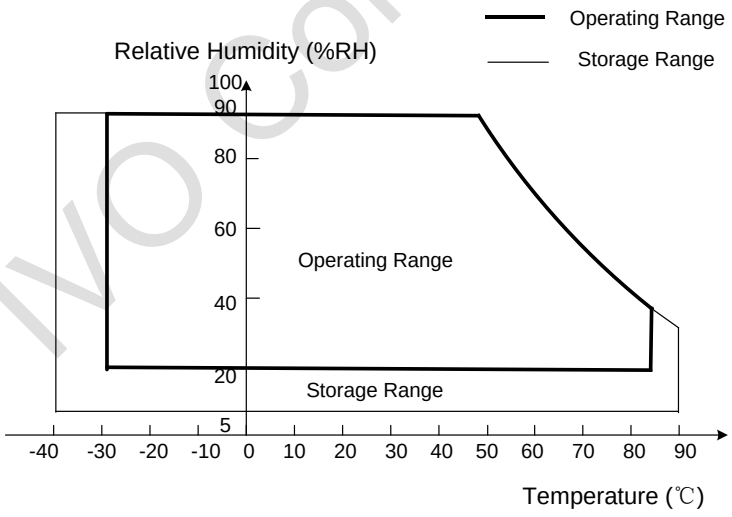
Note (3) (T<=40℃) Note static electricity. Maximum wet bulb temperature at 39℃ or less. (T>40℃) No condensation.

Note (4) There is a possibility of causing deterioration in the irregularity and others of the screen and the display fineness though the liquid crystal module doesn't arrive at destruction when using it at 85~90℃ or -40~-30℃.

Note (5) There is a possibility of causing the fineness deterioration by the prolonged use in the (high temperature) humidity environment (80%RH or more).

Note (6) In the operating temperature item, the low temperature side is the ambient temperature regulations. The high temperature side is the panel surface temperature regulations.

**Absolute Ratings of Environment of the LCD Module**



Note (7) half-sine; Frequency: 8Hz ~ 33Hz;Stroke: 1.3mm;Sweep: 2.9G 33.3Hz ~ 400Hz X,Z
Cycle : 15 minutes;2 hrs for each direction of X,Z ; 4 hours for Y direction
Note (8) 6ms, half sine wave, three times for X, Y, Z axis.

## 3.0 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes.

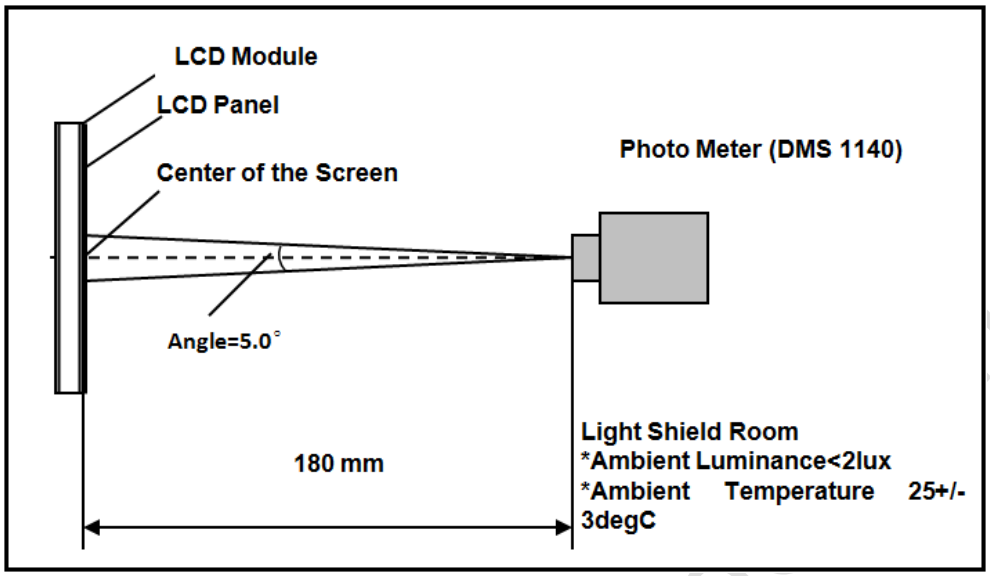
**Table 2 Optical Characteristics**

| Item | Conditions | | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| Viewing Angle （CR>10）☆ | Horizontal | $\theta_{x+}$ | 65 | 75 | - | degree | (1),(2),(3) |
| | | $\theta_{x-}$ | 65 | 75 | - | | |
| | Vertical | $\theta_{y+}$ | 60 | 70 | - | | |
| | | $\theta_{y-}$ | 65 | 75 | - | | |
| Contrast Ratio ☆ | Center | | 600 | 800 | - | - | (1),(2),(4) θx=θy=0° |
| Response Time | Rising + Falling | | - | 16 | 25 | ms | (1),(2),(5) θx=θy=0° |
| Color Chromaticity (CIE1931) ☆ | Red x | | Typ. -0.04 | 0.630 | Typ. +0.04 | - | (1),(2),(3) θx=θy=0° |
| | Red y | | | 0.358 | | - | |
| | Green x | | | 0.302 | | - | |
| | Green y | | | 0.641 | | - | |
| | Blue x | | | 0.150 | | - | |
| | Blue y | | | 0.059 | | - | |
| | White x | | | 0.315 | | - | |
| | White y | | | 0.335 | | - | |
| NTSC | - | | 67 | 72 | - | % | (1),(2),(3) θx=θy=0° |
| White Luminance ☆ | Center Point | | 550 | 670 | - | $cd/m^2$ | (1),(2),(6) θx=θy=0° |
| Luminance Uniformity | 9 Points | | 75 | 80 | - | % | (1),(2),(6) θx=θy=0° |

Note (1) Measurement Setup:

The LCD module should be stabilized at given temperature(25℃) for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.

**Figure 3 Measurement Setup**

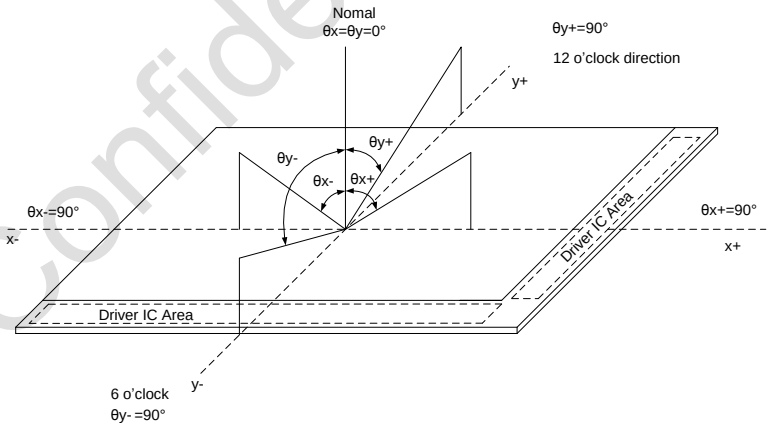



Note (2) The LED input parameter setting as:

I_LED: 420mA

Note (3) Definition of Viewing Angle

**Figure 4 Definition of Viewing Angle**




Note (4) Definition Of Contrast Ratio (CR)

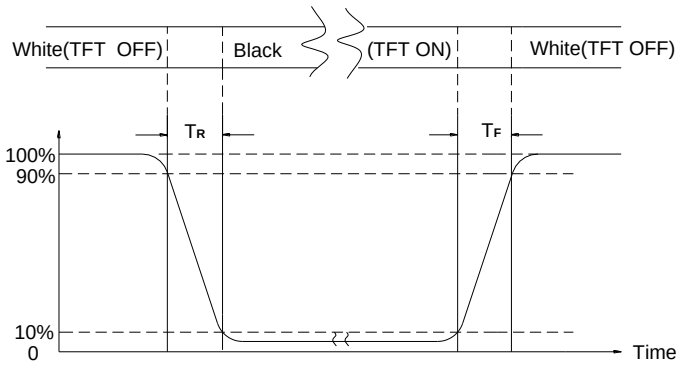
The contrast ratio can be calculated by the following expression:

Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255, L0: Luminance of gray level 0

Note (5) Definition Of Response Time ($T_R$, $T_F$)

**Figure 5 Definition of Response Time**



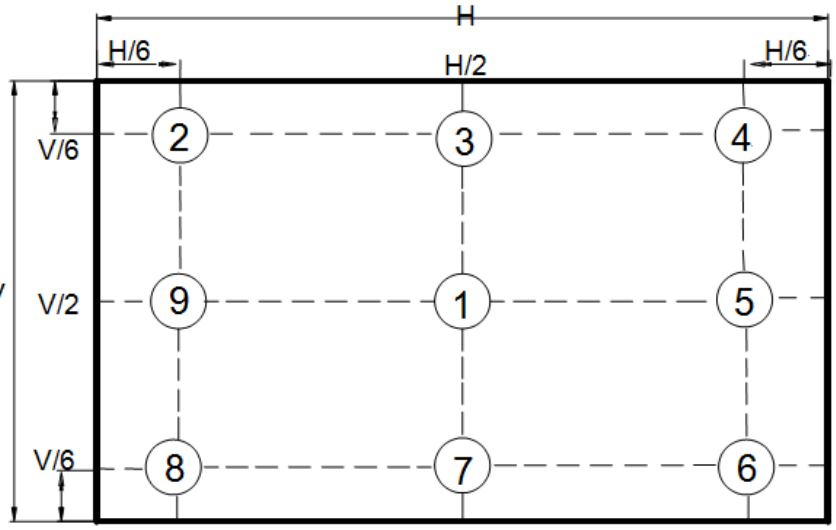

Note (6) Definition of Luminance Uniformity (Ref.: Active Area)

Measure the luminance of gray level 255 at 9 points.

Luminance Uniformity= Min.(L1, L2, ... L9) / Max.(L1, L2, ... L9)

H—Active Area Width, V—Active Area Height, L—Luminance

**Figure 6 Measurement Locations of 9 Points**



## 4.0 Electrical Characteristics

### 4.1 Interface Connector

**Table 3 Signal Connector Type**

| Item | Description |
|---|---|
| Manufacturer/Type | AORORA:F32D-1A7Y-21040 |

**Table 4 Signal Connector Pin Assignment**

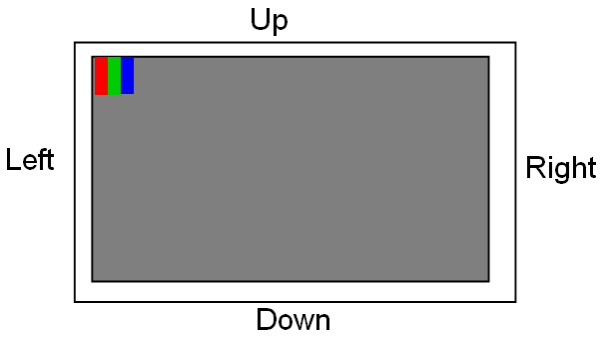
| Pin No. | Symbol | Description | Remarks |
|---|---|---|---|
| 1 | VCOM | Common voltage | |
| 2 | DVDD | Digital power | |
| 3 | DVDD | Digital power | |
| 4 | NC | Not connect | |
| 5 | RESET | Global reset pin. Active low to enter reset state.<br>Suggest to connecting with an RC reset circuit for stability.<br>Normally pull high.(R=10kΩ,C=1uF) | |
| 6 | STBYB | Standby mode ,normally pull high<br>STBYB ="1",normal operation<br>STBYB ="0",timing control ,source driver will turn off,all output are high-Z | |
| 7 | GND | Ground | |
| 8 | NIND0 | Negative LVDS differential data input | |
| 9 | PIND0 | Positive LVDS differential data input | |
| 10 | GND | Ground | |
| 11 | NIND1 | Negative LVDS differential data input | |

| | | | |
|---|---|---|---|
| 12 | PIND1 | Positive LVDS differential data input | |
| 13 | GND | Ground | |
| 14 | NIND2 | Negative LVDS differential data input | |
| 15 | PIND2 | Positive LVDS differential data input | |
| 16 | GND | Ground | |
| 17 | NINC | Negative LVDS differential clock input | |
| 18 | PINC | Positive LVDS differential clock input | |
| 19 | GND | Ground | |
| 20 | NIND3 | Negative LVDS differential data input | |
| 21 | PIND3 | Positive LVDS differential data input | |
| 22 | GND | Ground | |
| 23 | NC | Not connect | |
| 24 | NC | Not connect | |
| 25 | GND | Ground | |
| 26 | NC | Not connect | |
| 27 | NC | Not connect | |
| 28 | SELB | LVDS input data is 8 bits, SELB set to low | |
| 29 | AVDD | Power for Analog Circuit | |
| 30 | GND | Ground | |
| 31 | NC | Not connect | |

| | | | |
|---|---|---|---|
| 32 | NC | Not connect | |
| 33 | SHLR | Horizontal inversion | Note1 |
| 34 | UPDN | Vertical inversion | Note1 |
| 35 | VGL | Negative power for TFT | |
| 36 | NC | Not connect | |
| 37 | NC | Not connect | |
| 38 | VGH | Positive power for TFT | |
| 39 | NC | Not connect | |
| 40 | Bist | Normal operation/BIST pattern select. Normally pull low.<br>When BIST=H: BIST. (CLK input is not needed.)<br>When BIST=L: Normal operation. (Default) | System without the need to signal |

Note1：UPDN and SHLR control function

| SHLR | UPDN | Data shifting |
|---|---|---|
| DVDD | GND | Left→Right，Up→Down(default) |
| GND | GND | Right→Left，Up→Down |
| DVDD | DVDD | Left→Right，Down→Up |
| GND | DVDD | Right→Left，Down→Up |




**Power Supply Voltage**

| Item | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Avdd | 10.8 | 11.0 | 11.2 | V |
| Vcom | 4.0 | 4.2 | 4.4 | V |
| VGH | 19 | 20 | 21 | V |
| VGL | -7.8 | -6.8 | -5.8 | V |

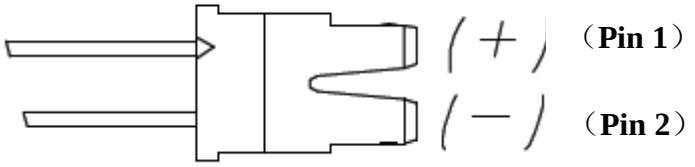
**Table 5 LED Connector Name / Designation**

| Item | Description |
|---|---|
| Manufacturer / Type | JST/BHSR-02VS-1 |
| Mating Receptacle / Type (Reference) | JST/SMO2B-BHSS-1 or Compatible |

**Table 6 LED Connector Pin Assignment**

| Pin No. | Symbol | Description | Remarks |
|---|---|---|---|
| 1 | A | Anode | + |
| 2 | K | Cathode | - |

**Figure 7 LED Connector**



### 4.2 Signal Electrical Characteristics

4.2.1 Signal Electrical Characteristics For LVDS Receiver

The built-in LVDS receiver is compatible with (ANSI/TIA/TIA-644 ) standard.

**Table 7 LVDS Receiver Electrical Characteristics**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Differential Input High Threshold | Vth | - | - | +100 | mV | $V_{CM}$=+1.2V |
| Differential Input Low Threshold | Vtl | -100 | - | - | mV | $V_{CM}$=+1.2V |
| Magnitude Differential Input Voltage | $\|V_{ID}\|$ | 200 | - | 600 | mV | - |
| Common Mode Voltage | $V_{CM}$ | 1.0 | 1.2 | 1.4 | V | $V_{th}$- $V_{tl}$ =200mA |
| Common Mode Voltage Offset | $\Delta V_{CM}$ | -50 | - | +50 | mV | $V_{th}$- $V_{tl}$ =200mA |

Note (1) Input signals shall be low or Hi- resistance state when VDD is off.

Note (2) All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD.

**Figure 8 Voltage Definitions**

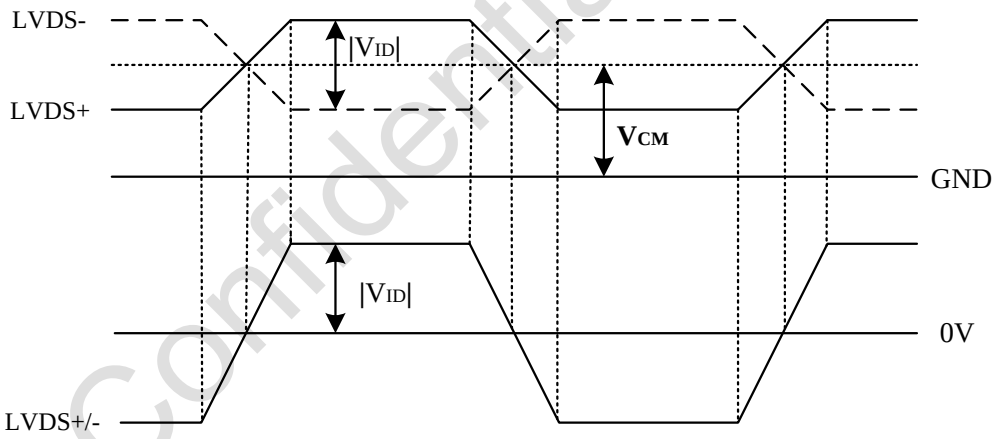


**Figure 9 Measurement System**

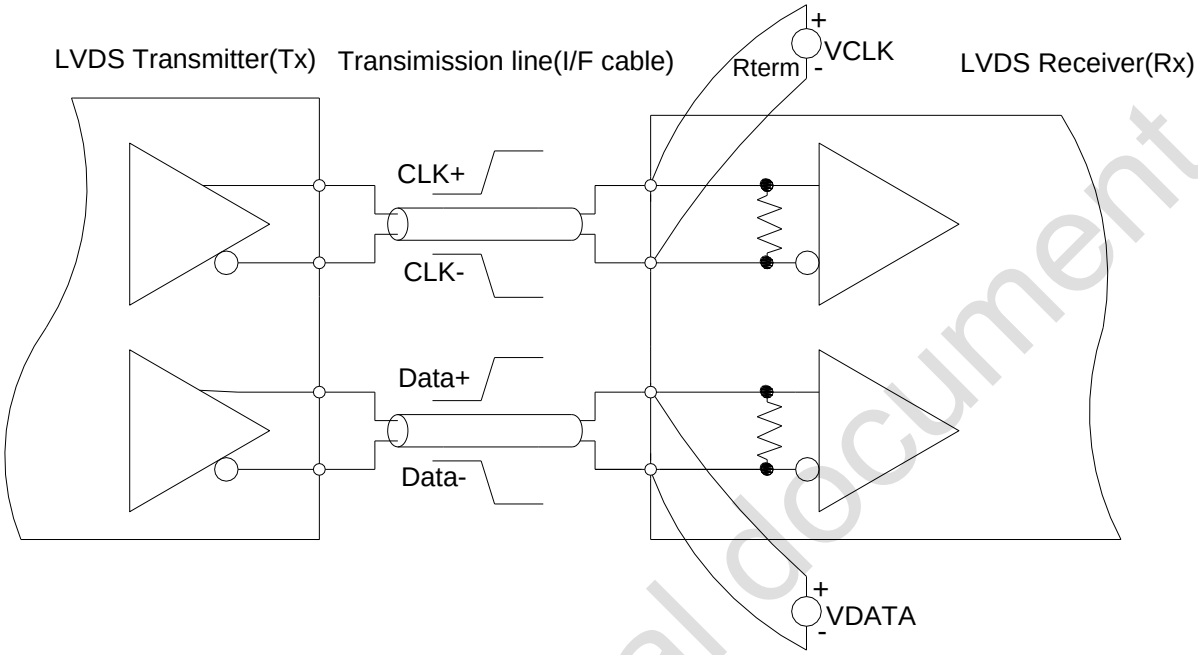
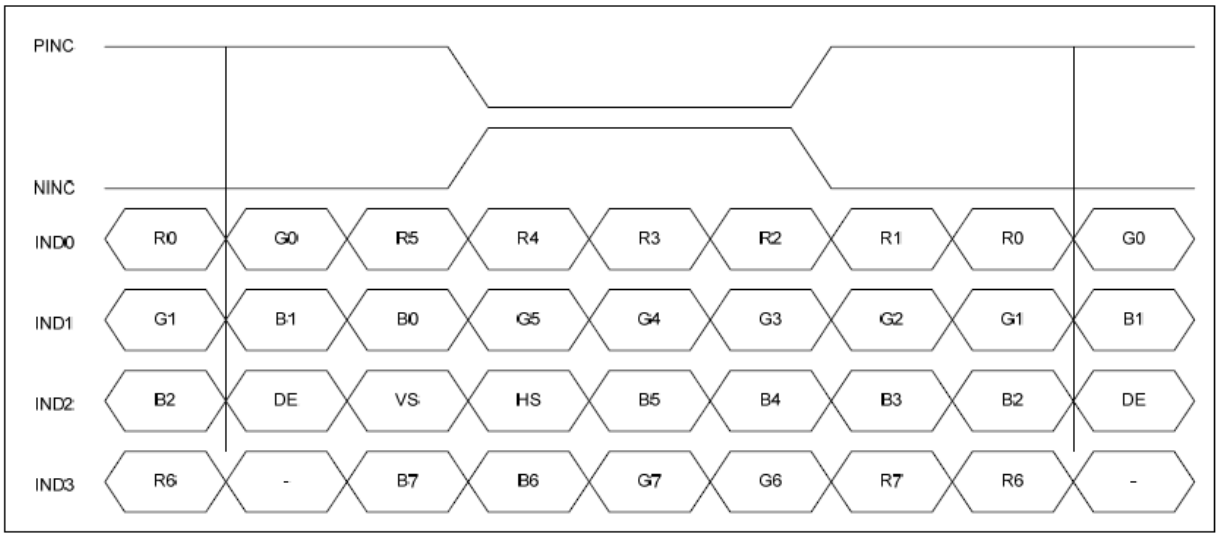



**Figure 10 Data Mapping**

Single 8 bit LVDS input

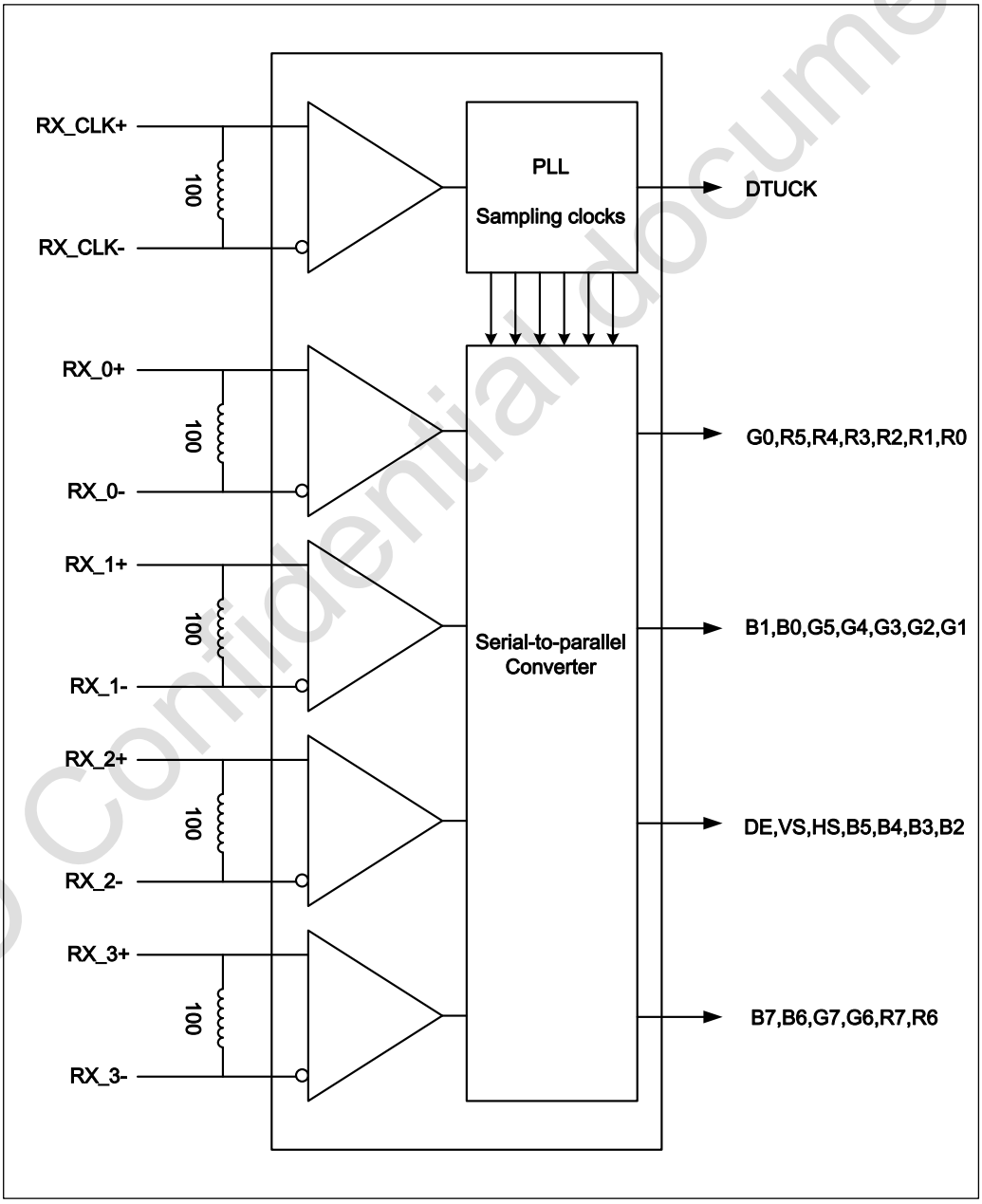


4.2.2 LVDS Receiver Internal Circuit

Figure 12 shows the internal block diagram of the LVDS receiver. This LCD module equips termination resistors for LVDS link.

**Figure 11 LVDS Receiver Internal Circuit**

8bit



### 4.3 Interface Timings

**Table 8 Interface Timings**

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| LVDS Clock Frequency | $f_{dck}$ | 45 | 51.2 | 57 | MHz |
| H Total Time | $T_{hp}$ | 1,324 | 1,344 | 1,364 | Clocks |
| H Active Time | HA | 1,024 | 1,024 | 1,024 | Clocks |
| H Blanking Time | $TH_{Blank}$ | 300 | 320 | 340 | Clocks |
| V Total Time | $T_{vp}$ | 625 | 635 | 645 | Lines |
| V Active Time | VA | 600 | 600 | 600 | Lines |
| V Blanking Time | $TV_{Blank}$ | 25 | 35 | 45 | Clocks |
| Frame Rate | $F_v$ | 50 | 60 | 65 | Hz |

### 4.4 Input Power Specifications

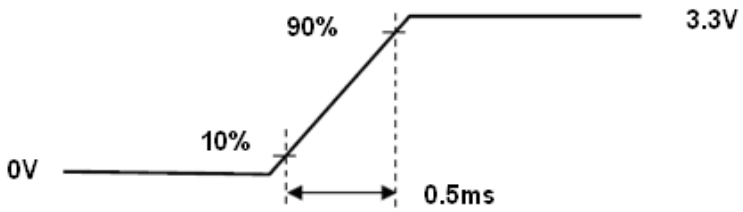
Input power specifications are as follows.

**Table 9 Input Power Specifications**

| Parameter | | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| **System Power Supply** | | | | | | | |
| LCD Drive Voltage (Logic) | | $D_{VDD}$ | 3.0 | 3.3 | 3.6 | V | (2), (4) |
| VDD Current | Black Pattern | $I_{DD}$ | - | - | 0.09 | A | (3),(4) |
| VDD Power Consumption | Black Pattern | $P_{DD}$ | - | - | 0.30 | W | |
| Rush Current | | $I_{Rush}$ | - | - | 1.5 | A | (1),(4),(5) |
| Allowable Logic/LCD Drive Ripple Voltage | | $V_{VDD-RP}$ | - | - | 200 | mV | (4) |
| **LED Power Supply** | | | | | | | |
| LED Input Voltage | | $V_{LED}$ | 8.4 | 9.6 | 10.2 | V | (4),(6) |
| LED Power Consumption | | $P_{LED}$ | - | - | 4.3 | W | (4),(6) |
| LED Forward Voltage | | $V_F$ | 2.8 | 3.2 | 3.4 | V | (4) |
| LED Forward Current | | $I_F$ | - | 60 | - | mA | |
| LED Life Time | | LT | 30,000 | - | - | Hours | (4)(7) |

Note (1) Measure Condition

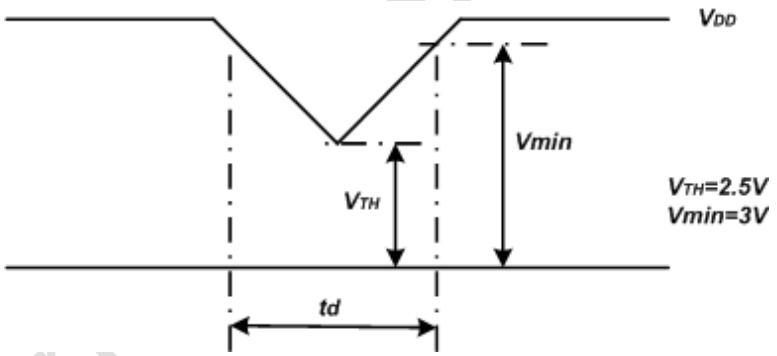
**Figure 12 VDD Rising Time**




Note (2) VDD Power Dip Condition

$V_{TH}$< $V_{DD}$≤ Vmin, td≤ 10ms (a time of the voltage return to normal), our panel can revive automatically.

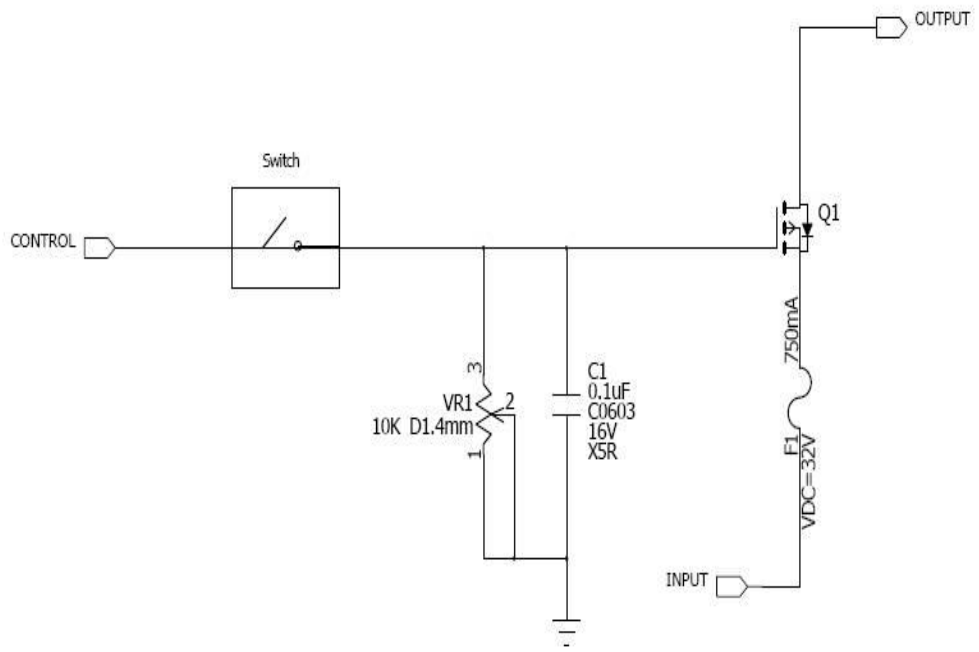
**Figure 13 VDD Power Dip**




Note (3) Frame Rate=60Hz, VDD=3.3V, DC Current.

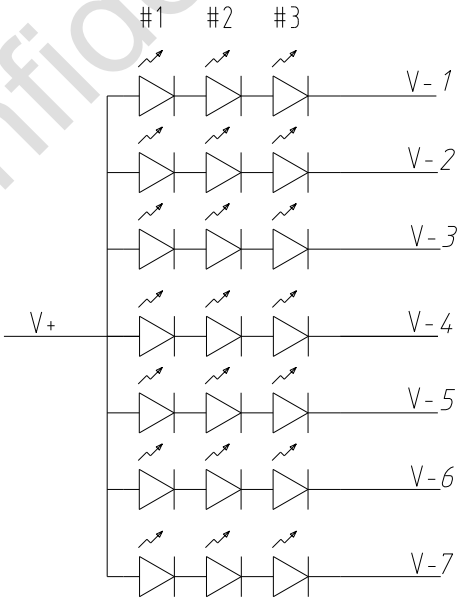
Note (4) Operating temperature 25℃, humidity 55%RH.

Note (5) The reference measurement circuit of rush current.




Note (6) Definition of $V_{LED}$ and $P_{LED}$

$V_{LED} = V_F \times 3$, $P_{LED} = V_{LED} \times I_F \times 7$

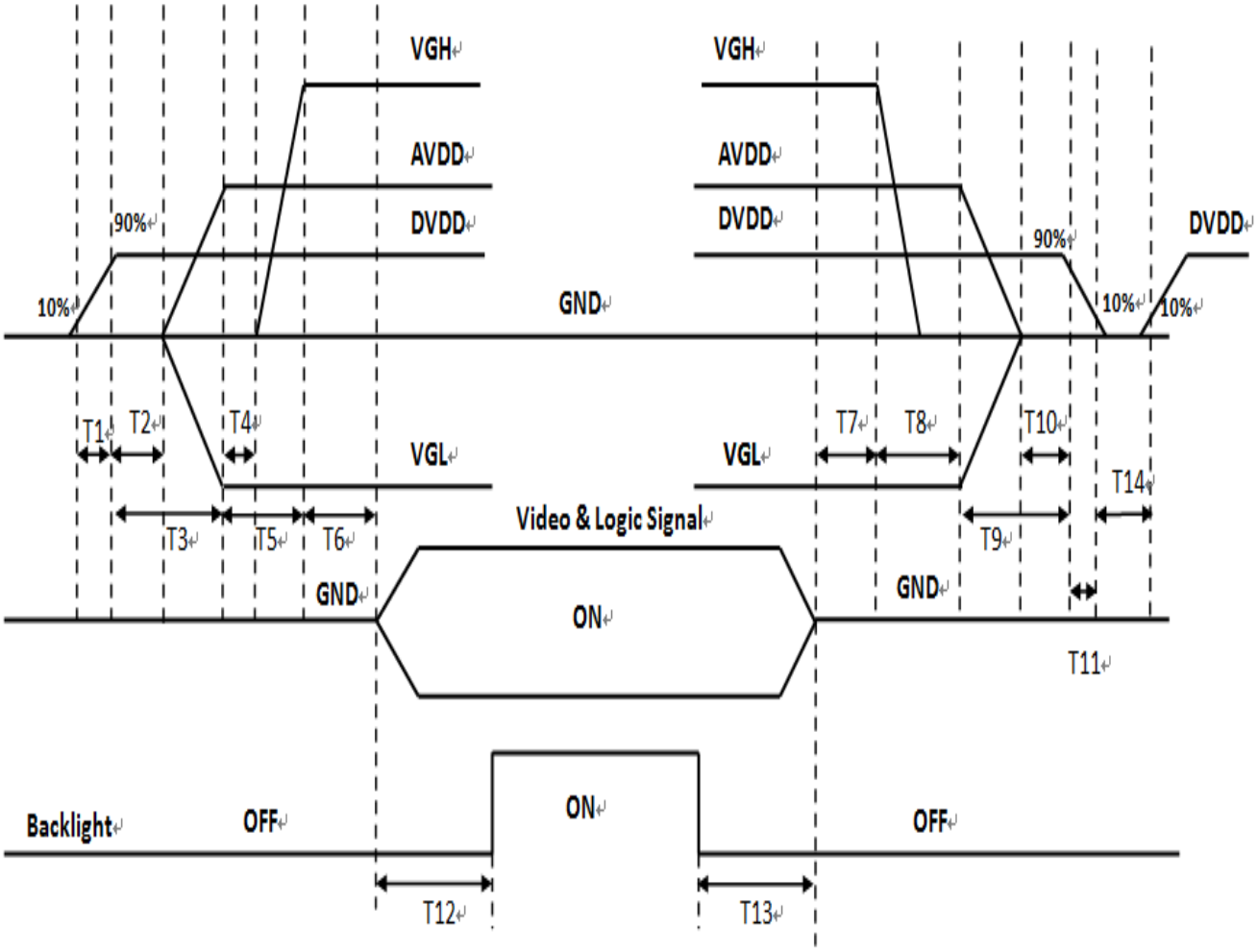



Note (7) The LED life time define as the estimated time to 50% degradation of initial luminous.

### 4.5 Power ON/OFF Sequence

Interface signals are also shown in the chart. Signals from any system shall be Hi- resistance state or low level when VDD voltage is off.

**Figure 14 Power Sequence**




Power On: DVDD→AVDD/VGL→VGH→Video & Logic Signal→Backlight

Power Off: Backlight→ Video & Logic Signal→ VGH→ AVDD/VGL→ DVDD

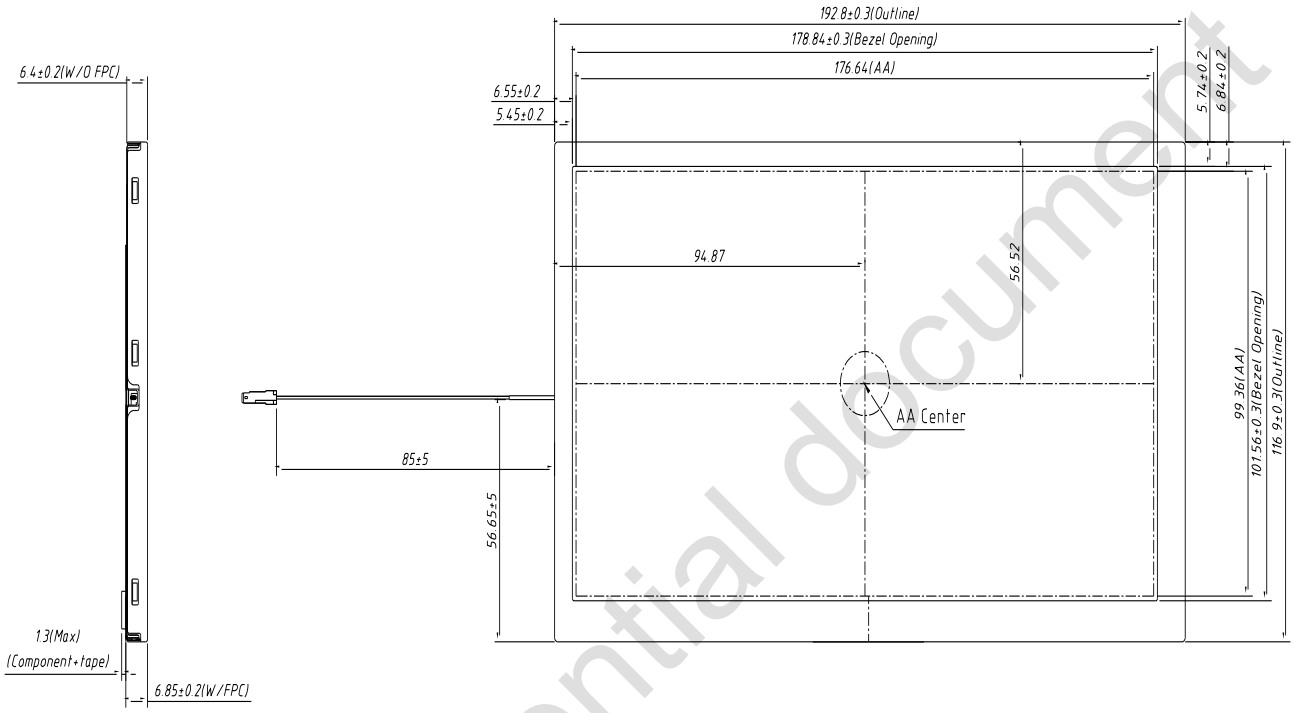
**Table 10 Power Sequencing Requirements**

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| DVDD Rising Time from 10% to 90% | T1 | 0.5 | - | 10 | ms |
| DVDD Good to AVDD/VGL On | T2 | 0 | - | - | ms |
| DVDD Good to AVDD/VGL Good | T3 | 20 | - | - | ms |
| AVDD/VGL Good to VGH On | T4 | 0 | - | - | ms |
| AVDD/VGL Good to VGH Good | T5 | 10 | - | - | ms |
| VGH Good to Signal Valid | T6 | 0 | - | 10 | ms |
| Signal Disable to VGH Down | T7 | 0 | - | 50 | ms |
| VGH Down to AVDD/VGL Down | T8 | 0 | - | 50 | ms |
| AVDD/VGL Down to DVDD Down | T9 | 0 | - | - | ms |
| AVDD/VGL Off to DVDD Down | T10 | 0 | - | - | ms |
| DVDD Falling Time | T11 | 0 | - | 10 | ms |
| Signal Valid to Backlight Power On | T12 | 200 | - | - | ms |
| Backlight Power Off to Signal disable | T13 | 200 | - | - | ms |
| Power Off Time | T14 | 500 | - | - | ms |

## 5.0 Mechanical Characteristics

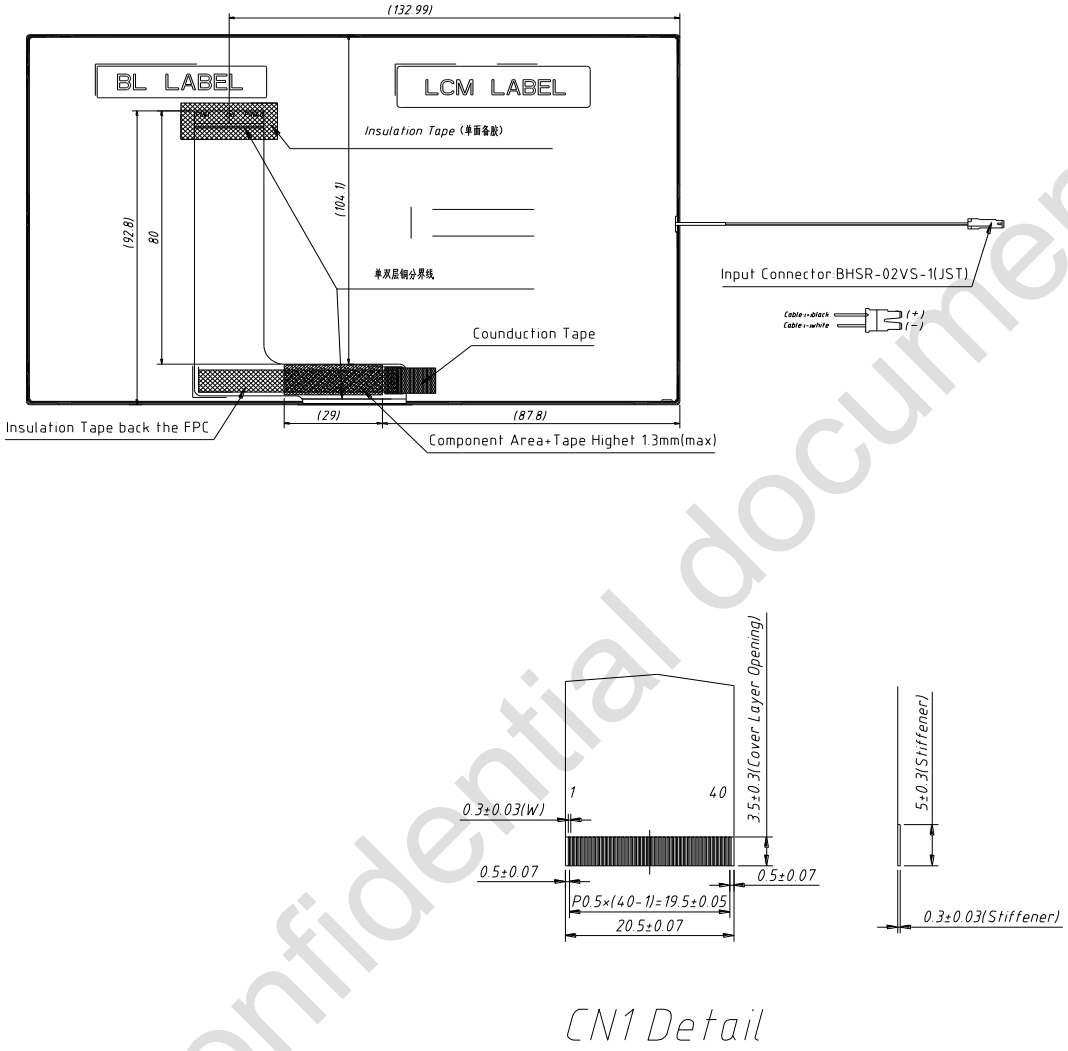
### 5.1 Outline Drawing

**Figure 15 Reference Outline Drawing (Front Side)**




**Note 1: Unnoted tolerance ±0.3**

**Figure 16 Reference Outline Drawing (Back Side)**

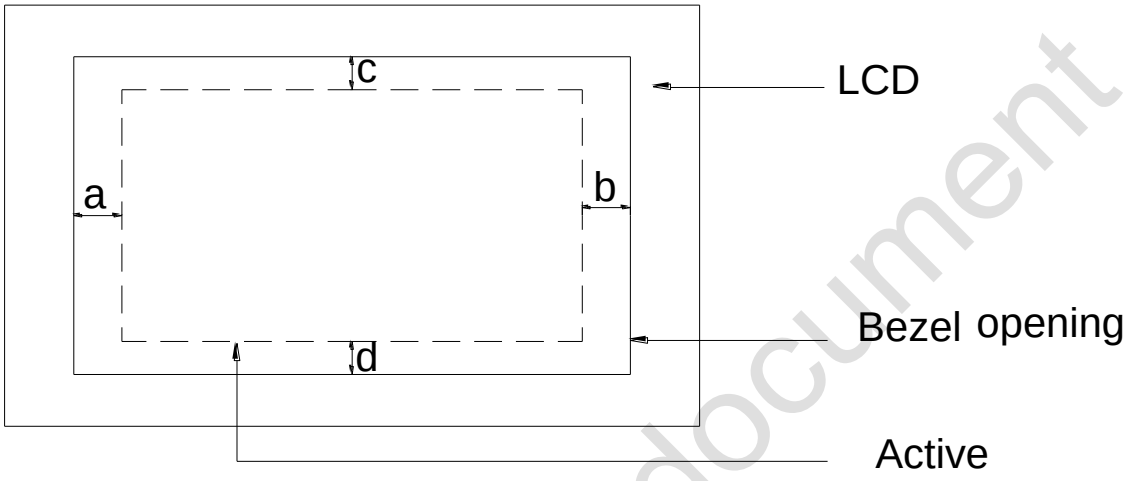



## 5.2 Dimension Specifications

**Table 11 Module Dimension Specifications**

| Item | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Width | 192.5 | 192.8 | 193.1 | mm |
| Height | 116.6 | 116.9 | 117.2 | mm |
| Thickness | 6.1 | 6.4 | 6.7 | mm |
| Weight | - | - | 240 | g |

**Figure 17 BM Area**




Note 1: a=b=c=d, 1.1mm

## 6.0 Reliability Conditions

| Item | | Package | Test Conditions | | Note |
|---|---|---|---|---|---|
| High Temperature Operating Test | | Module | 85℃, 500 hours | | (1),(2),(3),(4) |
| Low Temperature Operating Test | | Module | -30℃, 500 hours | | (1),(2),(3),(4) |
| High Temperature Storage Test | | Module | 90℃,500 hours | | (1),(2),(4) |
| Low Temperature Storage Test | | Module | -40℃, 500 hours | | (1),(2),(4) |
| High Temperature/High Humidity Operating Test | | Module | 65℃, 90%RH, 500 hours | | (1),(2),(3),(4) |
| High Temperature/High Humidity Storage Test | | Module | 65℃, 90%RH, 500 hours | | (1),(2),(3),(4) |
| Thermal Shock Storage | | Module | -40°(0.5hr)~85°(0.5hr)C/200cycles; | | (1),(2),(3),(4), Meet the system reaches 615cycles |
| ESD Test | Operating | Module | Contact | ±8KV,150pF(330Ohm)(Class B) | (5) |
| | | | Air | ±15KV,150pF(330 Ohm)(ClassB) | |

Note (1) All the judgments are under room temperature and the sample need to be static more than 2 hours in the room temperature before judge.

Note (2) During measurement, the condensation water or remains shall not be allowed.

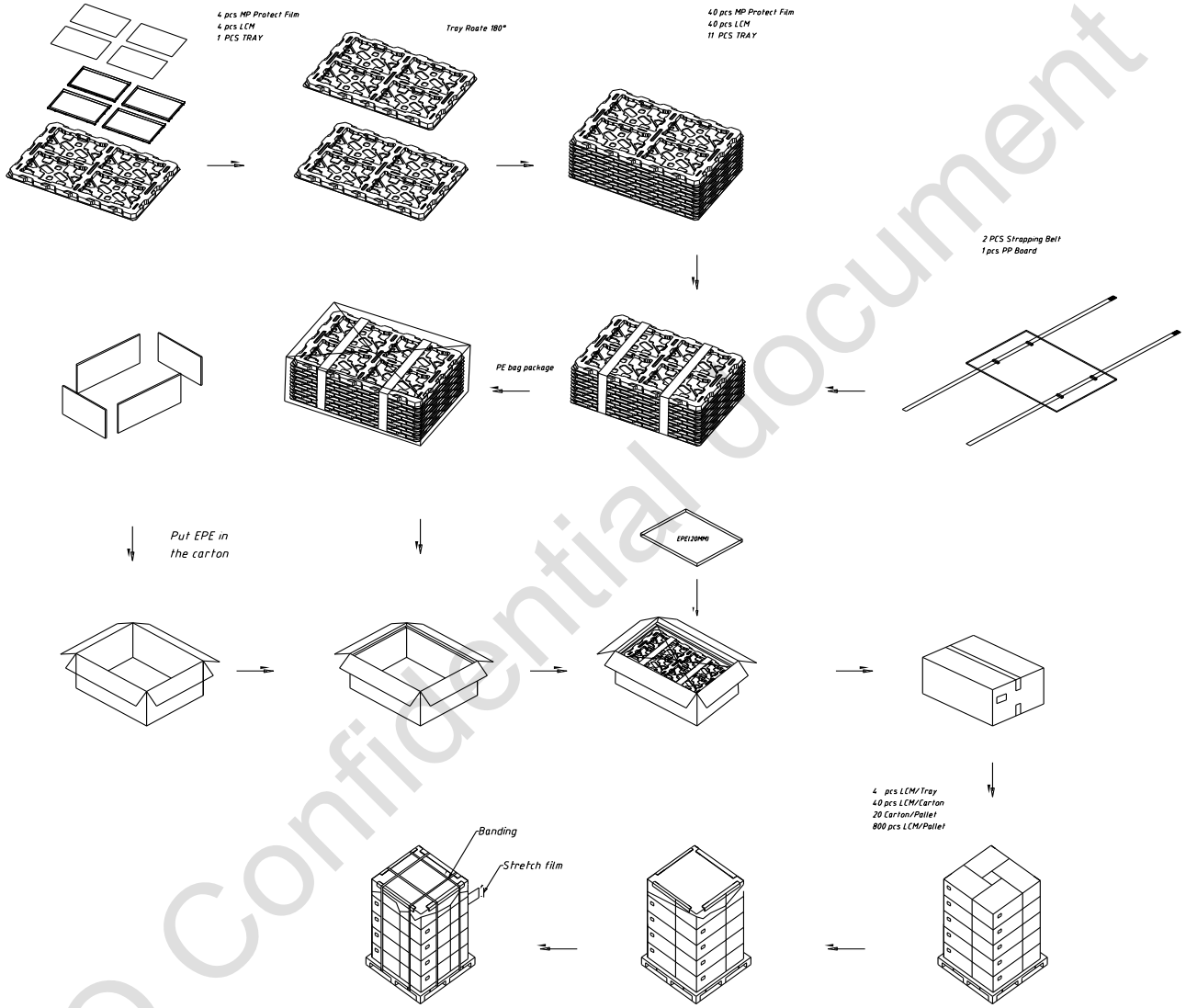
Note (3) In operating test, the backlight voltage and current must be in specification.

Note (4) There is no display function issue occurred, all the cosmetic specification is judged before the reliability stress.

Note (5) In case of malfunction defect caused by ESD damage. If it would be recovered to normal state after placing for a while, it would be judge as pass.

## 7.0 Package Specification

### Figure 18 Packing Method



## 8.0 Lot Mark


Note: This picture is only an example.

### 8.1 20 Lot Mark

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Code 1,2,4,5,6,7,8,9,10,11,16: IVO internal flow control code.
Code 3: Production Location.
Code 12: Production Year.
Code 13: Production Month.
Code 14,15: Production Day.
Code 17,18,19,20: Serial Number.

### 8.2 23 Product Barcode

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Code 1,2: Manufacture District.
Code 3,4,5,6,7: IVO internal module name.
Code 8,9,10,13,16: IVO internal flow control code.
Code 11,12: Cell location Suzhou, China defined as “KS”.
Code 14 ,15: Module location Kunshan, China defined as “KS”; Yangzhou, China defined as “YZ”; Shenzhen, China defined as “SE”; Zhuhai, China defined as “ZH”; Suzhou, China defined as “SZ”.
Code 17,18,19 : Year, Month, Day refer to Note(1), Note(2) and Note(3).
Note (1) Production Year

| Year | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | ..... | 2035 |
|---|---|---|---|---|---|---|---|---|---|---|
| Mark | 6 | 7 | 8 | 9 | A | B | C | D | ..... | Z |

Note (2) Production Month

| Month | Jan. | Feb. | Mar. | Apr. | May. | Jun. | Jul. | Aug. | Sep. | Oct | Nov. | Dec. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mark | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C |

Note (3) Production Day: 1~V.
Code 20~23 : Serial Number.

## 9.0 General Precaution

### 9.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

### 9.2 Handling Precaution

(1) Please mount LCD module by using mounting holes arranged in four corners tightly.
(2) Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. IVO does not warrant the module, if customers disassemble or modify the module.
(3) If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin. If liquid crystal contacts mouth or eyes, rinse out with water immediately. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.
(4) Disconnect power supply before handling LCD module.
(5) Refrain from strong mechanical shock and /or any force to the module.
(6) Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts parameters, environmental temperature; etc otherwise LCD module may be damaged. It's recommended employing protection circuit for power supply.
(7) Do not touch, push or rub the polarizer with anything harder than HB pencil lead. Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.
(8) When the surface is dusty, please wipe gently with absorbent cotton or other soft material. When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzene or other adequate solvent.
(9) Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.
(10) Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.
(11) Because LCD module uses CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge, please be careful with electrostatic discharge. Persons who handle the module should be grounded through adequate methods.
(12) Do not adjust the variable resistor located on the module.

### 9.3 Storage Precaution

(1) Please do not leave LCD module in the environment of high humidity and high temperature for a long time.
(2) The module shall not be exposed under strong light such as direct sunlight.Otherwise, display characteristics may be changed.
(3) The module should be stored in a dark place. It is prohibited to apply sunlight or fluorescent light in storage.

### 9.4 Operation Precaution

(1) Do not connect or disconnect the module in the "Power On" condition.

(2) Power supply should always be turned on/off by "Power On/Off Sequence".

(3) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference should be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

(4) After installation of the TFT module into an enclosure, do not twist nor bend the TFT module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT module from outside. Otherwise the TFT module may be damaged.

**9.5 Others**

(1) Ultra-violet ray filter is necessary for outdoor operation.

(2) Avoid condensation of water which may result in improper operation or disconnection of electrode.

(3) If the module keeps displaying the same pattern for a long period of time, the image may be "sticked" to the screen.

(4) This module has its circuitry PCB's on the rear side and should be handled carefully in order not to be stressed.

**9.6 Disposal**

When disposing LCD module, obey the local environmental regulations.