Document Title	P101GWWC R5 Tentative Product Specification			Page No.	1/35
Document No.		Issue date	2020/05/29	Revision	00

Tentative Product Specification

To:

Product Name: P101GWWC R5

Document Issue Date: 2020/05/29

Customer	InfoVision Optoelectronics
SIGNATURE _____ _____ _____ Please return 1 copy for your confirmation with your signature and comments.	**SIGNATURE** **REVIEWED BY CQM** _____ **PREPARED BY FAE** _____

Note : 1. Please contact InfoVision Company before designing your product based on this product.
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FQ-7-30-0-009-03D

Revision	Date	Page	Revised Content/Summary	Remark
00	2020/05/29	--	First issued.	

CONTENTS

1.0 General Descriptions

1.1 Introduction

The M101GWWC R5 is a Color Active Matrix Liquid Crystal Display. The matrix uses a-Si Thin Film Transistor as a switching device. This TFT LCD has a 10.1 inch diagonally measured active display area with WXGA resolution (800 horizontal by 1,280 vertical pixels array).

1.2 Features

- Supported WXGA Resolution
- MIPI Interface
- Wide View Angle
- Compatible with RoHS Standard

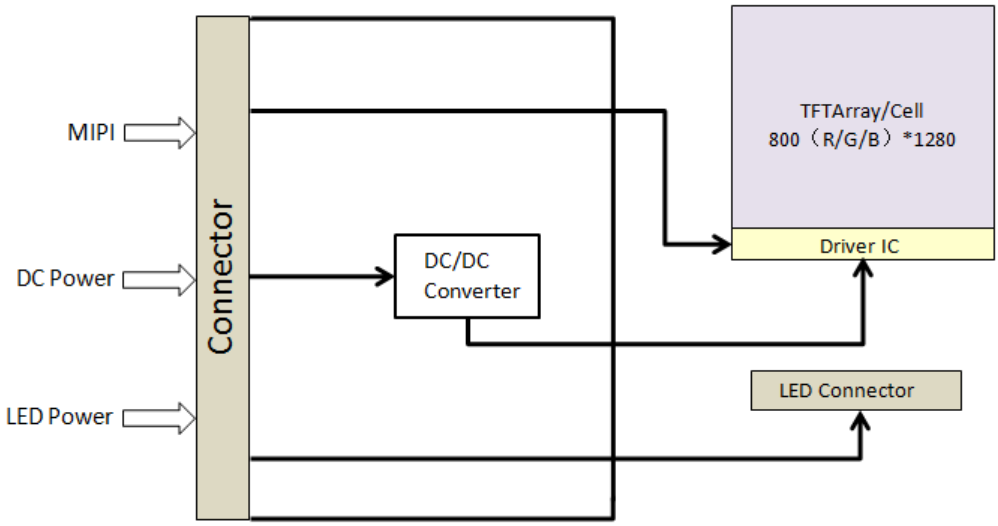
1.3 Product Summary

Items	Specifications	Unit
Screen Diagonal	10.1	inch
Active Area (H x V)	135.36×216.58	mm
Number of Pixels (H x V)	800×1,280	-
Pixel Pitch (H x V)	0.1692×0.1692	mm
Pixel Arrangement	R.G.B. Vertical Stripe	-
Display Mode	Normally Black	-
Contrast Ratio	(1000) (Typ.)	-
Response Time	(30) (Typ.)	ms
Input Voltage	3.3 (Typ.)	V
Power Consumption	(0.4) (Max.)@White Pattern ,FV=60Hz	W
Weight	(85) (Max.)	g
Outline Dimension(Without PCBA)	(139.36) (Typ.) × (225.8) (Typ.) × (1.75) (Max.)	mm
Outline Dimension(With PCBA)	(139.36) (Typ.) × (252.658) (Typ.) × (1.75) (Max.)	mm
Electrical Interface (Logic)	MIPI	-
Support Color	16.7 M	-
NTSC	(60) (Typ.)	%
Surface Treatment	Anti-glare	-
Transmittance	(6.2) (Typ.)	

1.4 Functional Block Diagram

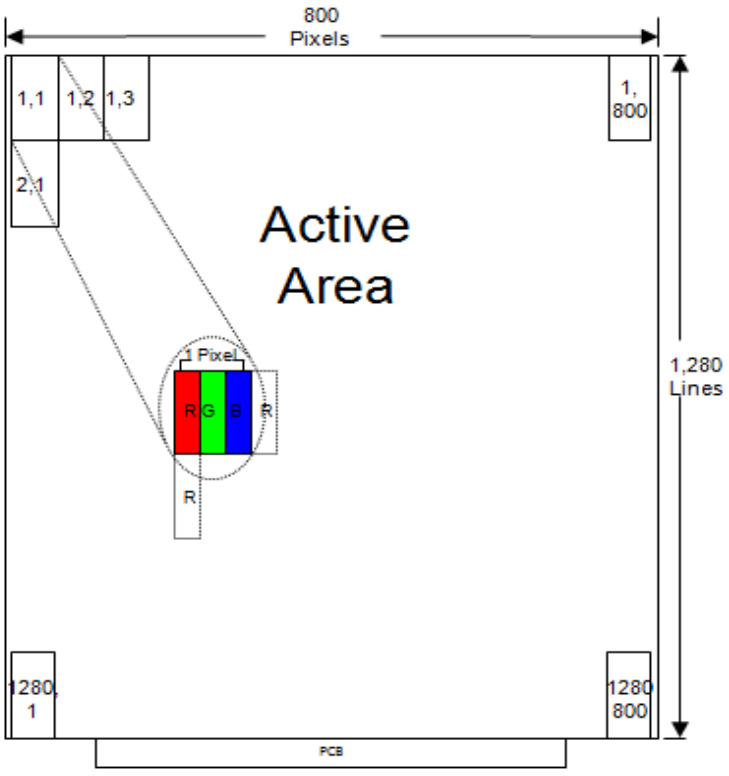
Figure 1 shows the functional block diagram of the LCD open-cell.

Figure 1 Block Diagram



1.5 Pixel Mapping

Figure2 Pixel Mapping



2.0 Absolute Maximum Ratings

Table 1 Electrical & Environment Absolute Rating

Item	Symbol	Min.	Max.	Unit	Note
Logic Supply Voltage	V_{DD}	（-0.3）	（6.0）	V	(1),(2),(3),(4)
Logic Supply Voltage	Iovcc	（-0.3）	（3.6）	V	
Operating Temperature	T_{gs}	0	50	℃	
Storage Temperature	T_a	-20	60	℃	

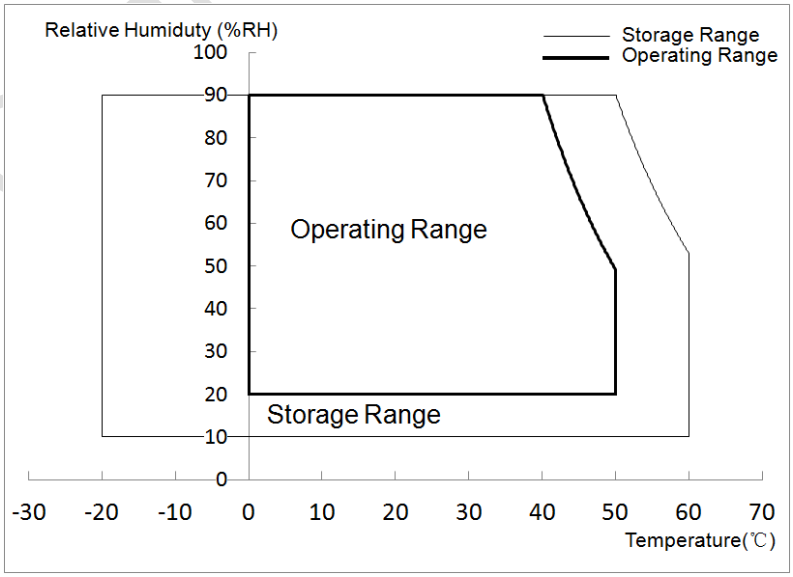
Note (1) All the parameters specified in the table are absolute maximum rating values that may cause faulty operation or unrecoverable damage, if exceeded. It is recommended to follow the typical value.

Note (2) All the contents of electro-optical specifications and display fineness are guaranteed under Normal Conditions. All the display fineness should be inspected under normal conditions. Normal conditions are defined as follow: Temperature: 25℃, Humidity: 55± 10%RH.

Note (3) Unpredictable results may occur when it was used in extreme conditions. T_a= Ambient Temperature, T_{gs}= Glass Surface Temperature. All the display fineness should be inspected under normal conditions.

Note (4) Temperature and relative humidity range are shown in the figure below. Wet bulb temperature should be lower than 38.3℃, and no condensation of water. Besides, protect the module from static electricity.

Figure 3 Absolute Ratings of Environment of the LCD open-cell



3.0 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes.

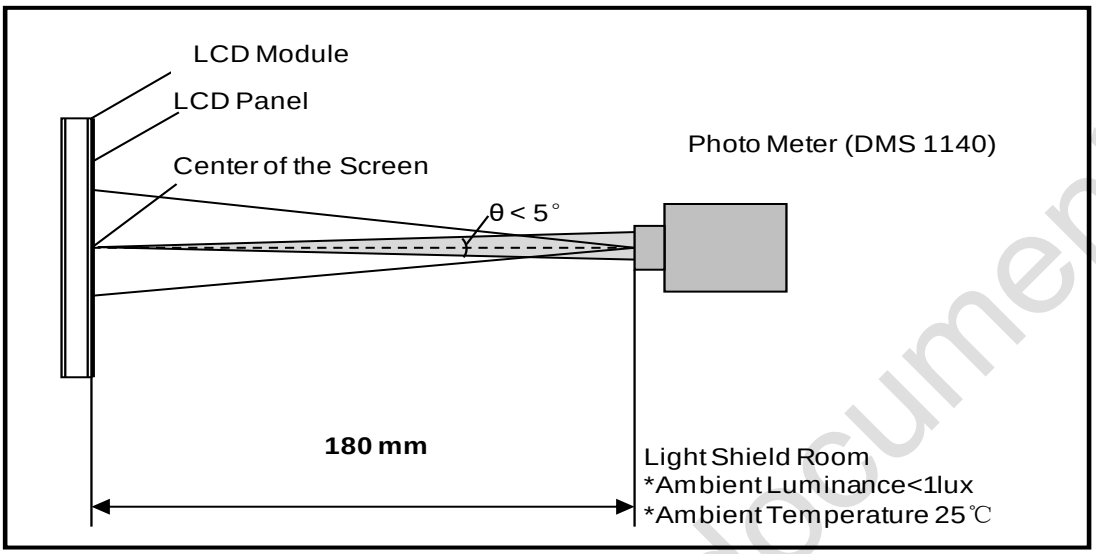
Table 2 Optical Characteristics

Item	Conditions		Min.	Typ.	Max.	Unit	Note
Viewing Angle （CR≥10）	Horizontal	θ_{x+}	(80)	(85)	-	degree	(1),(2),(3),(6),(7)
		θ_{x-}	(80)	(85)	-		
	Vertical	θ_{y+}	(80)	(85)	-		
		θ_{y-}	(80)	(85)	-		
Contrast Ratio	Center		(800)	(1,000)	-	-	(1),(3),(6),(7) θx=θy=0°
Response Time	Rising + Falling		-	(30)	(35)	ms	(1),(4),(6),(7) θx=θy=0°
Color Chromaticity (CIE1931)	Red x		Typ. -0.03	(0.619)	Typ. +0.03	-	(1),(6),(7) θx=θy=0°
	Red y			(0.361)		-	
	Green x			(0.342)		-	
	Green y			(0.606)		-	
	Blue x			(0.149)		-	
	Blue y			(0.102)		-	
	White x			(0.300)		-	
	White y			(0.320)		-	
NTSC	-		(55)	(60)	-	%	
Transmittance	-		(5.8)	(6.2)	-	%	(1),(5),(7),(8) θx=θy=0°

Note (1) Measurement Setup:

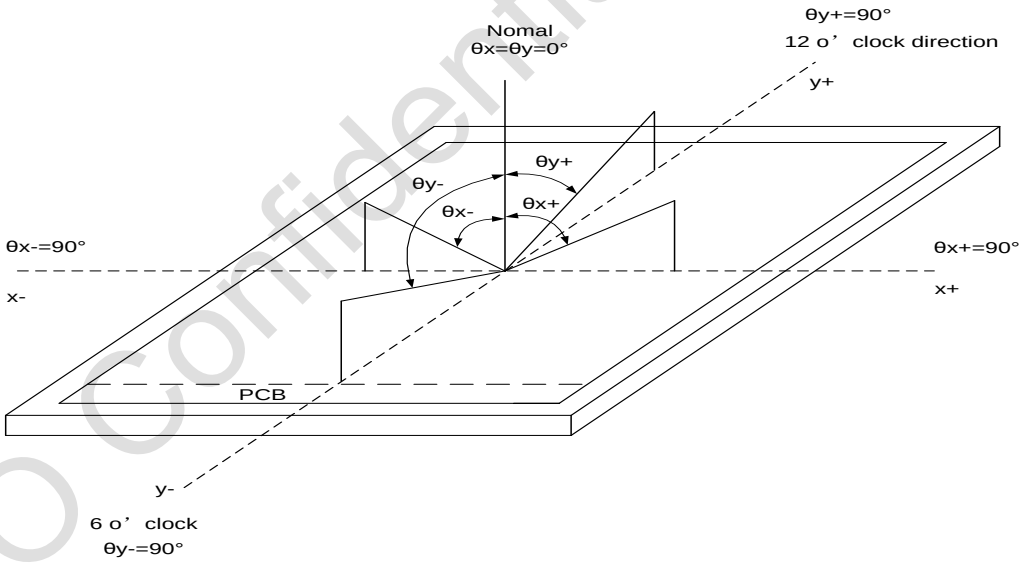
The LCD module should be stabilized at given ambient temperature (25℃) for 30 minutes to avoid abrupt temperature changing during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 30 minutes in the windless room.

Figure 4 Measurement Setup



Note (2) Definition of Viewing Angle

Figure 5 Definition of Viewing Angle



Note (3) Definition of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression:

Contrast Ratio (CR) = White / Black

Note (4) Definition of Response Time (T_R, T_F)

Figure 6 Definition of Response Time

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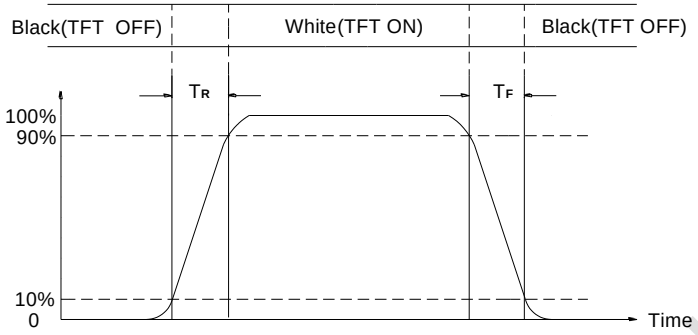
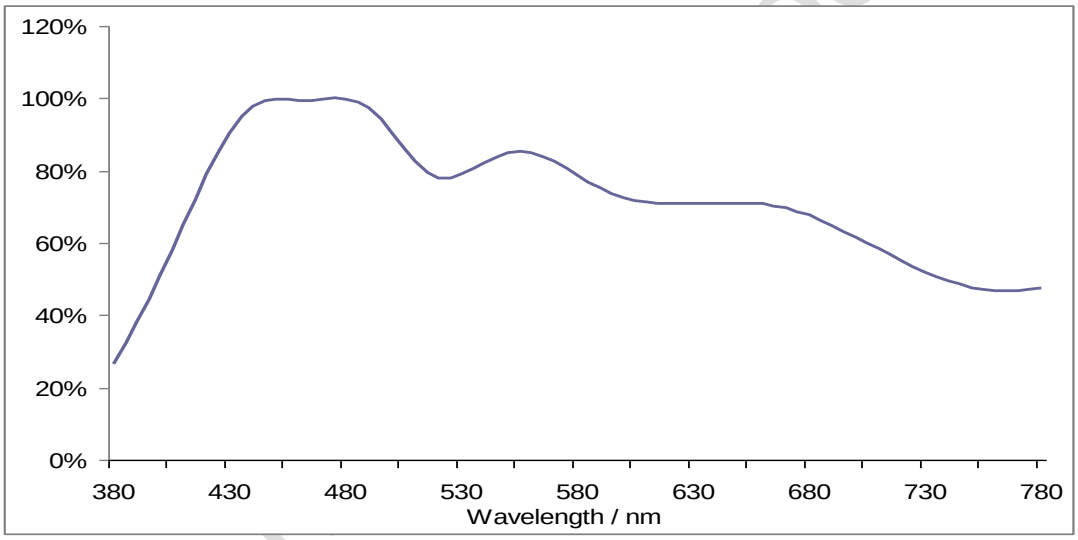


Note (5) C-Light Spectrum

Figure 7 C-Light Spectrum



Note (6) Light source is the BL which is supplied by IVO-TBD

Note (7) All optical data are based on IVO given system & nominal parameter & testing machine in this document.

Note (8) Definition of Transmittance

$$\text{Transmittance} = \frac{\text{Center Luminance of LCD}}{\text{Center Luminance of Back Light}} \text{ X100\%}$$

4.0 Electrical Characteristics

4.1 Interface Connector

Table 3 Signal Connector Type

Item	Description
Manufacturer / Type	Hirose/FH26W-39S-0.3SHW(60)

Table 4 Signal Connector Pin Assignment

Pin No	Symbol	Description	Remarks
1	NC	NC	-
2	NC	NC	-
3	NC	NC	-
4	FB4	LED-	-
5	FB3	LED-	-
6	FB2	LED-	-
7	FB1	LED-	-
8	NC	NC	-
9	VLED	LED+	-
10	VLED	LED+	-
11	VLED	LED+	-
12	VPP	External high voltage pin, used in OTP mode and operates at 7.5v, If not used, let it open	-
13	NC	NC	-
14	NC	NC	-
15	GND	GND	-
16	LCD_RST	Reset	-
17	SCL	I2C-Compatible Serial-Clock Input of Digital Vcom (Only Use for IVO)	-
18	SDA	I2C-Compatible Serial-Data Input/output of Digital Vcom (Only Use for IVO)	-
19	VDD	3.3V	-
20	VDD	3.3V	-
21	VDD	3.3V	-
22	IOVCC	1.8V	-
23	IOVCC	1.8V	-
24	GND	GND	-

25	D3P	MIPI Input Data Pair D3P	-
26	D3N	MIPI Input Data Pair D3N	-
27	GND	GND	-
28	D2P	MIPI Input Data Pair D2P	-
29	D2N	MIPI Input Data Pair D2N	-
30	GND	GND	-
31	CLKP	MIPI Input Data Pair CLKP	-
32	CLKN	MIPI Input Data Pair CLKN	-
33	GND	GND	-
34	D1P	MIPI Input Clock Pair D1P	-
35	D1N	MIPI Input Clock Pair D1N	-
36	GND	GND	-
37	D0P	MIPI Input Clock Pair D0P	-
38	D0N	MIPI Input Clock Pair D0N	-
39	GND	GND	-

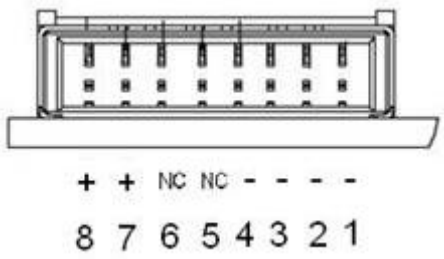
Table 5 LED Connector Name / Designation

Item	Description
Manufacturer / Type	Starconn/ 6700S08-000000-G2-R

Table 6 LED Connector Pin Assignment

Pin No.	Symbol	Description	Remarks
1	FB1	LED cathode voltage1	-
2	FB2	LED cathode voltage2	-
3	FB3	LED cathode voltage3	-
4	FB4	LED cathode voltage4	-
5	NC	NC	-
6	NC	NC	-
7	VOUT	LED anode voltage	-
8	VOUT	LED anode voltage	-

Figure 8 LED Connector



4.2 Signal Electrical Characteristics

4.2.1 Reset Input Timing

Figure 9 Reset input timings

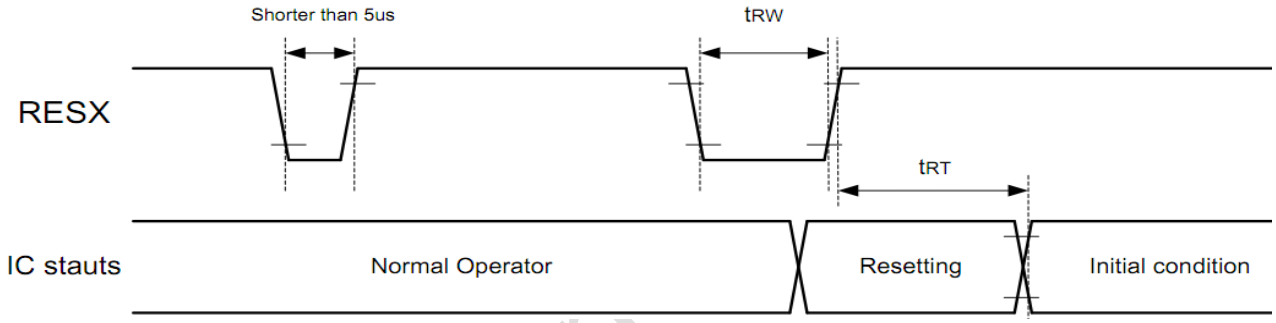


Table 7 Signal of Reset input timings

Symbol	Parameter	Related pins	Min	Max	Unit	Note
tRW	Reset pulse width(2)	RESX	10	-	μs	-
tRT	Reset complete time(3)	-	-	5	ms	(5)
		-	-	120	ms	(6),(7)

Note (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done everytime when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

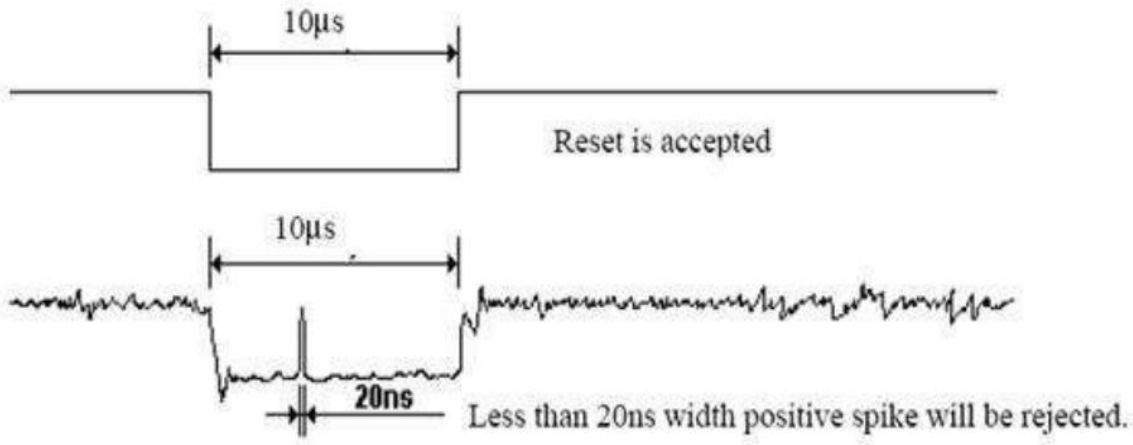
Table 8 Spike of RESX line

RESX Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out–mode. The display remains the blank state in Sleep In–mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:

Figure 10 Reset timings



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out Command, it is necessary to wait 120msec then send RESX.

4.2.2 DSI D-PHY electronic characteristics

The Description of D-PHY Layer In general, the DSI - PHY may contain the following electrical functions: Low-Power Receiver (LP-RX), High-Speed Receiver (HS-RX), the Low-Power. Contention Detector (LP-CD), and Low Power Transmitter (LP-TX). Figure 10 shows the complete

set of electronic functions required for a fully featured PHY transceiver.

Figure 11 Electronic functions of a D-PHY transceiver

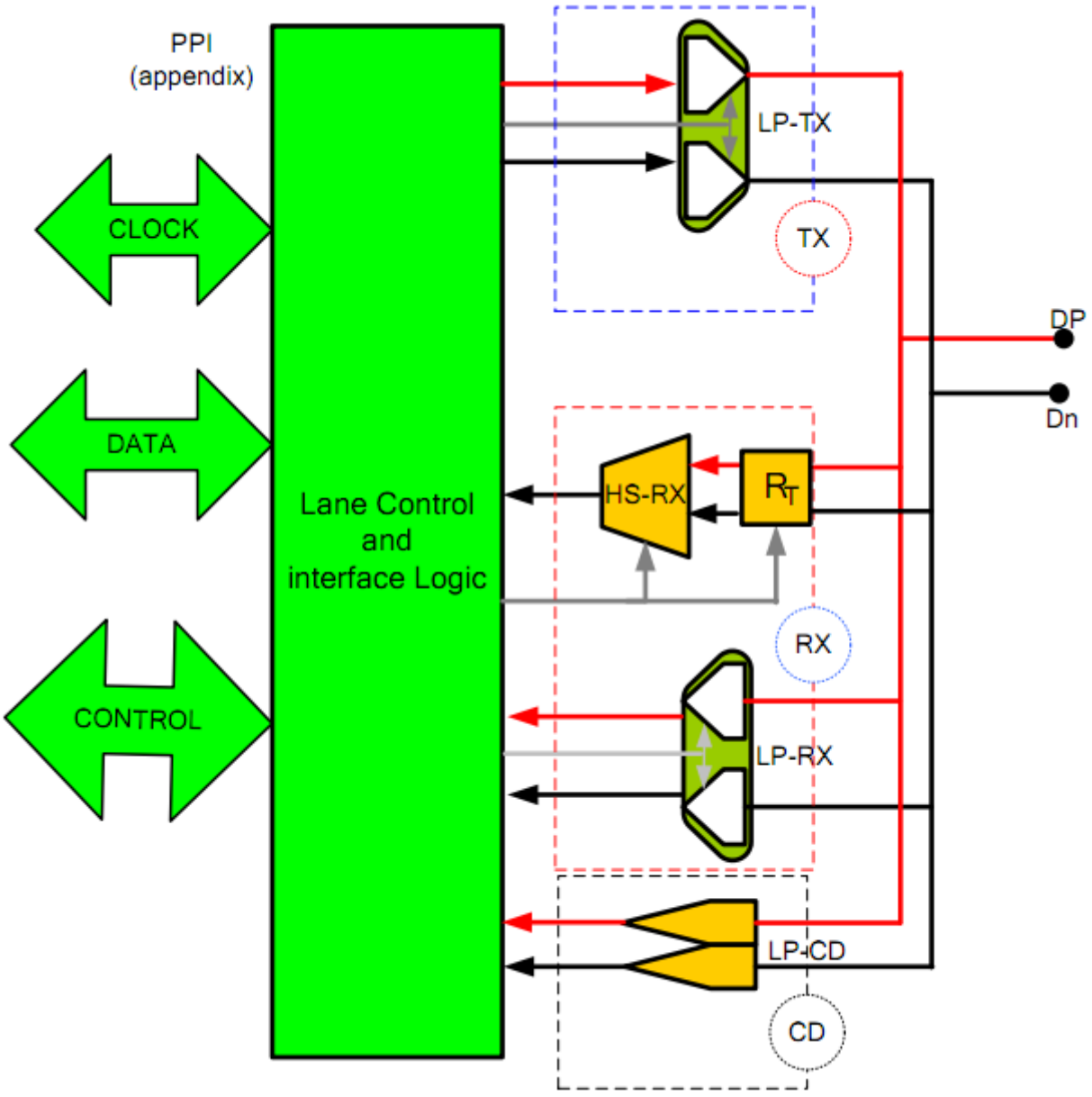
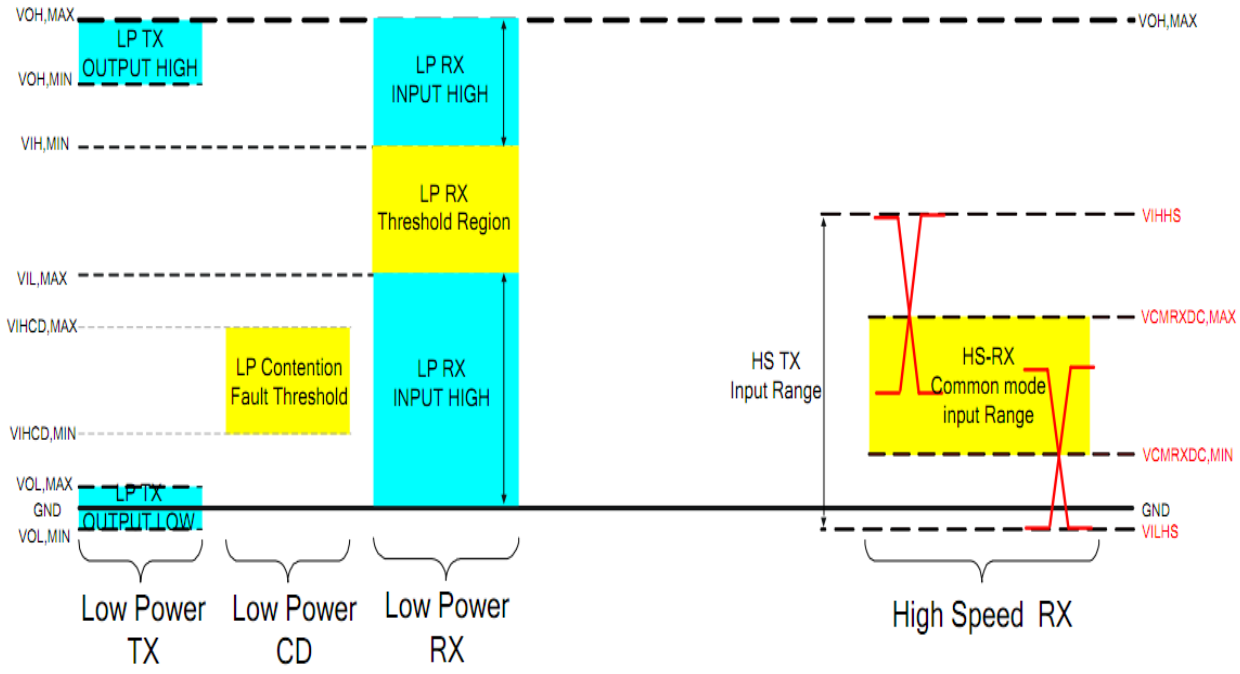


Figure12 shows both the HS and LP signal levels of electronic characteristics, respectively. Where, the HS receiver utilizes low-voltage swing differential signaling. The LP transmitter and LP receiver utilize low-voltage swing single signaling. Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed

mode during normal operation.

Figure 12 HS and LP signal levels



4.2.3 The Electronic Characteristics of Low-Power Transmitter (TX)

The Low-Power TX shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power modes. Hence, it is important to keep static power consumption of a LP TX be as low as possible. Under tables list DC and AC characteristic for Low power transmitter.

Table 9 LP-TX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
VOH	Thevenin output high level	1.1	1.2	1.3	V	-
VOL	Thevenin output low level	-50	-	50	mV	-
ZOLP	Output impedance of LP-TX	110	-	-	Ω	(1)

Note (1) Though no maximum value for ZOLP is specified, the LP transmitter output impedance shall ensure the tRLP / tFLP specification is met.

Table 10 LP-TX AC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
tRLP/tFLP	15%-85% rise time and fall time	-	-	25	ns	(1)
TLP-PER-TX	Period of the LP exclusive-OR clock	90	-	-	ns	-
δV/δtSR	Slew rate @ CLOAD = 0pF	30	-	500	mV/ns	(1), (3),(5),(6)
	Slew rate @ CLOAD = 5pF	-	-	300	mV/ns	(1), (3),(5),(6)
	Slew rate @ CLOAD = 20pF	-	-	250	mV/ns	(1), (3),(5),(6)
	Slew rate @ CLOAD = 70pF	-	-	150	mV/ns	(1), (3),(5),(6)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1), (3),(7)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30 – 0.075 *(VO,INST-700)	-	-	mV/ns	(1), (8),(9)
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1), (2),(3)
CLOAD	Load capacitance	-	-	70	pF	-

Note (1) CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

(2) When the output voltage is between 400 mV and 930 mV.

(3) Measured as average across any 50 mV segment of the output signal transition.

(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.

(5) This value represents a corner point in a piecewise linear curve.

(6) When the output voltage is in the range specified by VPIN(absmax).

(7) When the output voltage is between 400 mV and 700 mV.

(8) Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.

(9) When the output voltage is between 700 mV and 930 mV.

4.2.4 Signal Electrical Characteristics For MIPI Receiver

The Electronic Characteristics of Receiver (RX)

This part includes two parts which Low-Power RX and High-Speed RX. Because they have differential DC and AC characteristic, first to describe LP-RX then describe HS-RX.

Low-Power Receiver (RX)

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSPIKE. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The Figure 13 shows Input Glitch Rejection of Low-Power RX. In addition, under tables list DC and AC characteristic for LP-RX.

Figure 13 Input Glitch Rejections of Low-Power Receivers

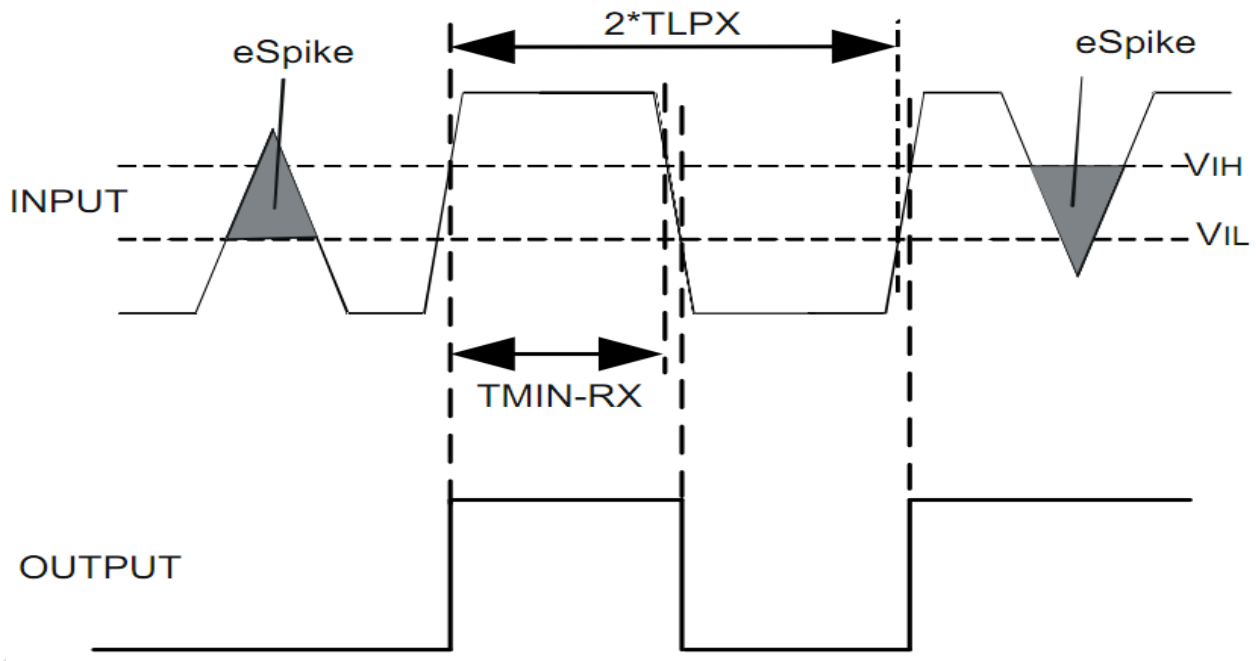


Table 11 LP-RX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
VIH	Logic 1 input threshold	880	-	-	mV	-
VIL	Logic 0 input threshold, not in ULP state	-	-	550	mV	-

Table 12 LP-RX AC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
eSPIKE	Input pulse rejection	-	-	300	V.ps	(1),(2),(4)
TMIN	Minimum pulse width response	20	-	-	ns	(4)
VINT	Peak-to-peak interference voltage	-	-	200	mV	-
fINT	Interference frequency	450	-	-	MHz	-

Note (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state

(2) An impulse less than this will not change the receiver state.

(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

(4) An input pulse greater than this shall toggle the output.

Line Contention Detection

Contention can be inferred by following conditions:

1. Detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than VIL.

2. Detect an LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than VIHCD.

Table 13 Contention Detector DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
VIHCD	Logic 1 contention threshold	450	-	-	mV	-
VILCD	Logic 0 contention threshold	-	-	200	mV	-

High-Speed Receiver (RX)

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, ZID, between the positive input pin Dp and the negative input pin Dn. Under Tables list DC and AC characteristic for HS-RX.

Table 14 HS Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
VCMRXDC	Common-mode voltage HS receive mode	70	-	330	mV	(1),(2)
VIDTH	Differential input high threshold	-	-	70	mV	-
VIDTL	Differential input low threshold	-70	-	-	mV	-
VIHHS	Single-ended input high voltage	-	-	460	mV	(1)
VILHS	Single-ended input low voltage	-40	-	-	mV	(1)
ZID	Differential input impedance	80	100	125	Ω	-

Note (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz.

Table 15 HS Receiver AC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
ΔVCMRX(HF)	Common mode interference beyond 450 MHz	-	-	100	mVpp	(1)
CCM	Common mode termination	-	-	60	pF	(2)

Note (1) ΔVCMRX(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.

(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

4.2.5 MIPI Data-Clock Timing

Figure 14 MIPI Data-Clock Timing Definitions

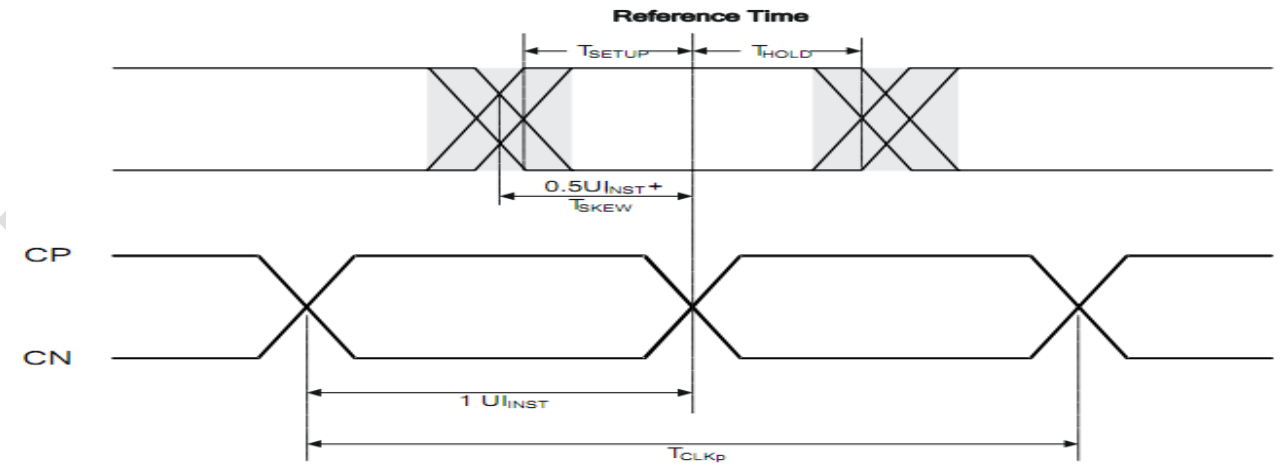


Table16 MIPI Data-Clock Timing Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	-	-	12.5	ns	(1),(2),(3) (4),(5),(6)
Date to Clock Setup Time(Receiver)	T_{SETUP}(RX)	(0.15)	-	-	UI_{INST}	(7),(8)
Clock to Date Hold Time (Receiver)	T_{HOLD}(RX)	(0.15)	-	-	UI_{INST}	(7), (8)

Note (1) This value corresponds to a minimum 80 Mbps data rate.

(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

(3) Maximum total bit rate is 850Mbps of 1 data lane 24-bit data format.

(4) Maximum total bit rate is 1.7Gbps of 2 data lanes 24-bit data format.

(5) Maximum total bit rate is 2Gbps of 3 data lanes 24-bit data format.

(6) Maximum total bit rate is 2Gbps of 4 data lanes 24-bit data format.

(7) Total setup and hold window for receiver of 0.3 UI_{INST}.

(8) T_{SETUP} (RX) and T_{HOLD} (RX) are only RX without PCB and connector and guaranteed by design.

4.2.6 Burst Mode Data Transmission

Figure 15 High-Speed Data Transmission in Bursts

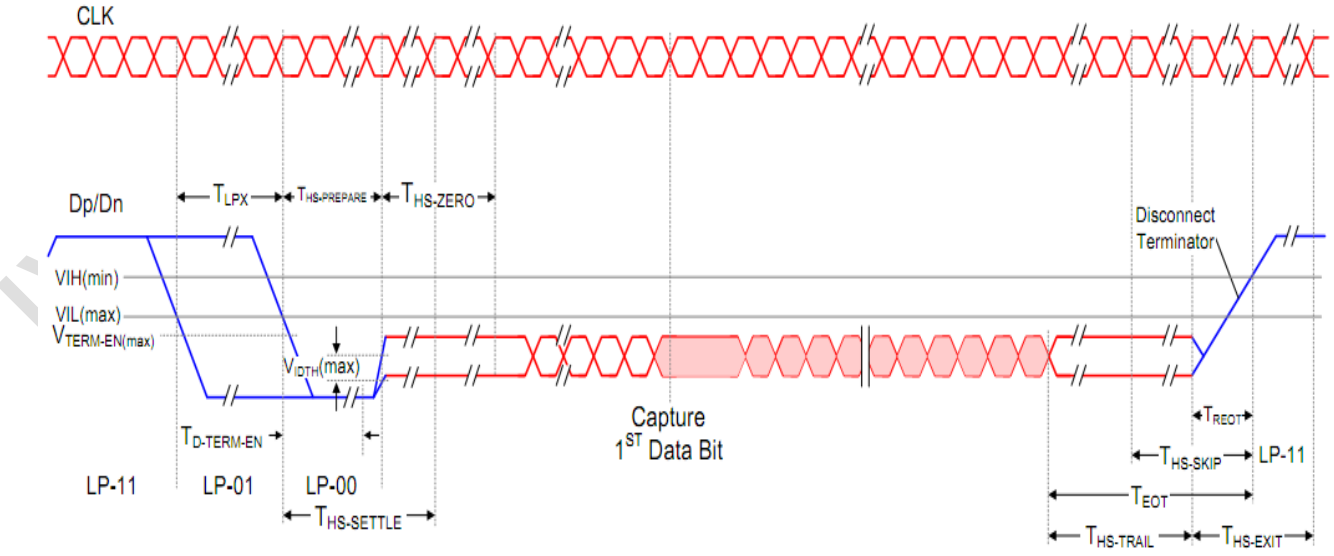


Table17 Signal of High-Speed Data

Parameter	Description	Min.	Typ.	Max.	Unit
TLPX	Transmitted length of any Low-Power state period.	50	-	-	ns
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	40+4*UI	-	85+6*UI	ns
THS-PREPARE +THS-ZERO	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145+10* UI	-	-	ns
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination.	-	-	35+4*UI	ns
THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85+6*UI	-	145 + 10*UI	ns
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	max(n*8 *UI,60+n *4*UI)	-	-	ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

Figure 16 Switching the Clock Lane between Clock Transmission and Low-Power Mode

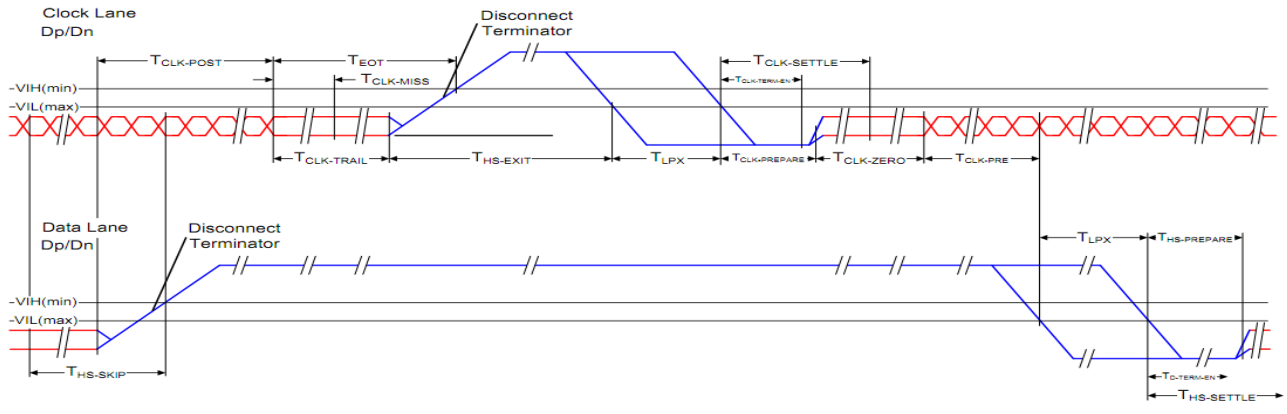


Table18 Signal of Switching

Parameter	Description	Min.	Typ.	Max.	Unit
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60+52 *UI	-	-	ns
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	-	ns
TCLK-PREPARE +TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
THS-EXIT	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	100	-	-	ns

4.3 Interface Timings

Table 19 Interface Timings

Parameter	Symbol	Unit	Min.	Typ.	Max.
DCLK	fdck	MHz	-	(69)	-
H Total Time	Th	clocks	-	(872)	-
H Active Time	HA	clocks		800	
H Front Porch	Thf	clocks	-	(32)	-
H Pulse Width	THP	clocks	-	(20)	-
H Back Porch	Thb	clocks	-	(20)	-
V Total Time	Tv	lines	-	(1312)	-
V Active Time	VA	lines		1280	
V Front Porch	Tvf	lines	-	(16)	-
V Pulse Width	TVP	lines	-	(3)	-
V Back Porch	Tvb	lines	-	(12)	-
V Frequency	fv	Hz	-	（60）	-

Note: Htotal*Vtotal*Frame Frequency≤69 MHz

4.4 Input Power Specifications

Input power specifications are as follows.

Table 20 Input Power Specifications

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
System Power Supply							
LCD Drive Voltage (Logic)		V_{DD}	3.0	3.3	3.6	V	(1),(2)
VDD Current	White Pattern	I_{DD}	-	-	（0.121）	A	(1),(2),(3)
VDD Power Consumption	White Pattern	P_{DD}	-	-	（0.4）	W	
Input Power Supply Voltage		IOVCC	-	(1.8)	-	V	
Input Power Supply Current		IIN	-	-	(0.03)	A	
Input Power Supply Voltage		VPP	(7.25)	(7.5)	(7.75)	V	
Rush Current		I_{Rush}	-	-	（1.0）	A	(1),(4)
Allowable Logic/LCD Drive Ripple Voltage		V_{VDD-RP}	-	-	（200）	mV	(1)

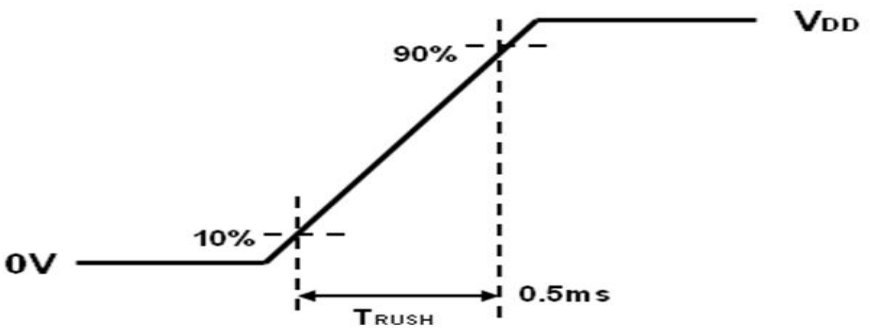
Note (1) All of the specifications are guaranteed under normal conditions. Normal conditions are defined as follow: Temperature: 25℃, Humidity: 55± 10%RH.

Note (2) All of the absolute maximum ratings specified in the table, if exceeded, may cause faulty operation or unrecoverable damage. It is recommended to follow the typical value.

Note (3) The specified V_{DD} current and power consumption are measured under the V_{DD} = 3.3 V, F_V = 60 Hz condition and White Pattern.

Note (4) The figures below is the measuring condition of V_{DD}. Rush current can be measured when T_{RUSH} is 0.5 ms.

Figure 17 V_{DD} Rising Time



4.5 Power ON/OFF Sequence

1.Interface signals are also shown in the chart. Signals from any system shall be Hi-resistance state or low level when VDD voltage is off.

2. When system first start up, should keep the VDD high time longer than 200ms, otherwise may cause image sticking when VDD drop off.

Figure 18 Power On Sequence

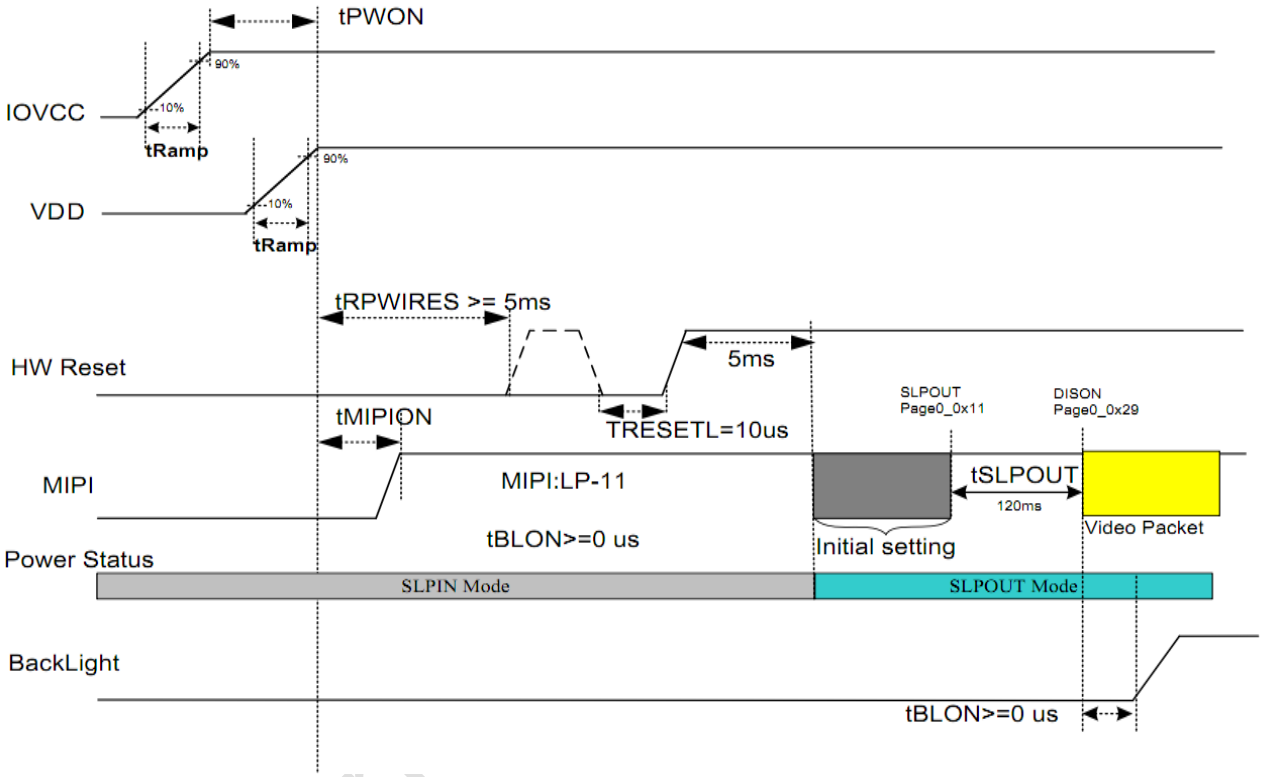
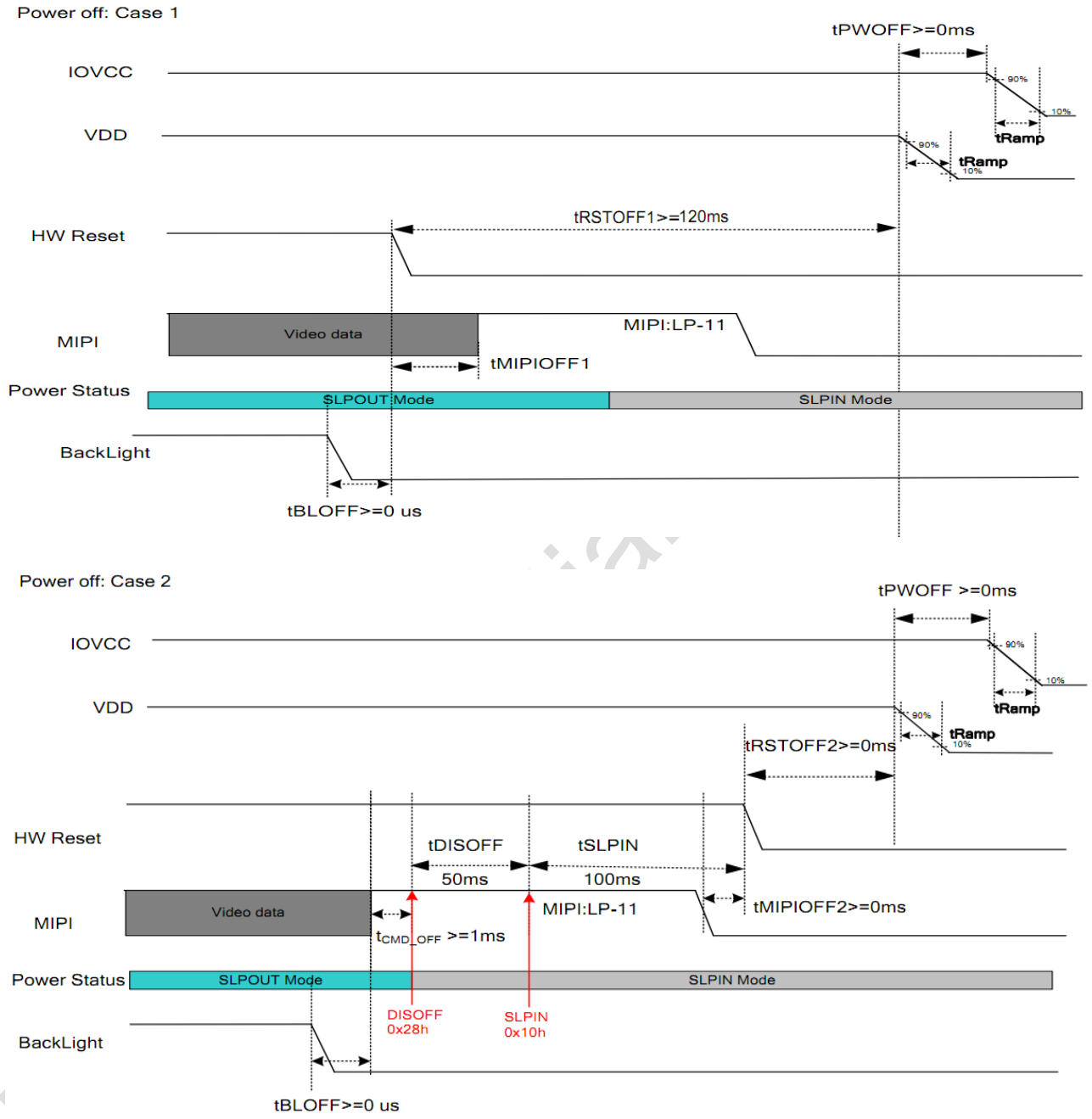


Table 21 Power On Sequencing Requirements

Symbol	Min	Typ	Max	Unit
tRamp	-	no limit	-	us
tPWON	(0)	-	-	ms
tMIPI-ON	(0)	-	tRPWIRES	ms
tRPWIRES	(5)	-	-	ms
tRESETL	(10)	-	-	ms
tSLPOUT	(120)	-	-	ms
tBLON	(0)	-	-	ms

Figure 19 Power Off Sequence



Note: For the power off case2, DISOFF command and tDISOFF are optional. That means t_{CMD_OFF} could be followed by the SLPIN command an tSLPIN, without DISOFF command and tDISOFF.

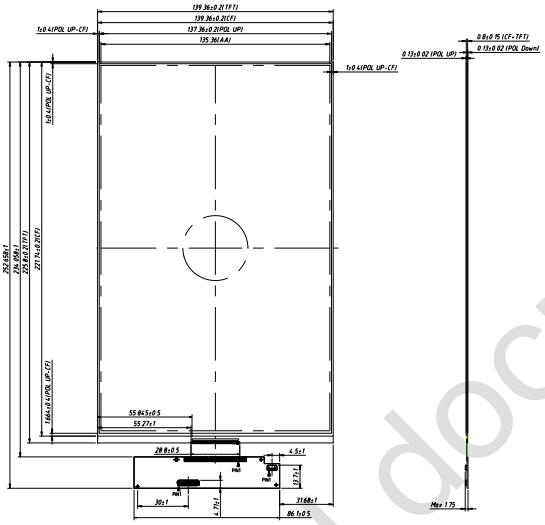
Table 22 Power Off Sequencing Requirements

Symbol	Min	Typ	Max	Unit	Remark
tRamp	-	no limit	-	us	
tPWONFF	(0)	-	-	ms	
tMIPIOFF1	(0)	-	-	ms	power off case1
tMIPIOFF2	(0)	-	-	ms	power off case2
tRSTOFF2	(0)	-	-	ms	power off case2
tRSTOFF1	(120)	-	-	ms	power off case1
tCMD_OFF	(1)	-	-	ms	power off case2
tDISOFF	(50)	-	-	ms	power off case2
tSLPIN	(100)	-	-	ms	power off case2
tBLOFF	(0)	-	-	ms	

5.0 Mechanical Characteristics

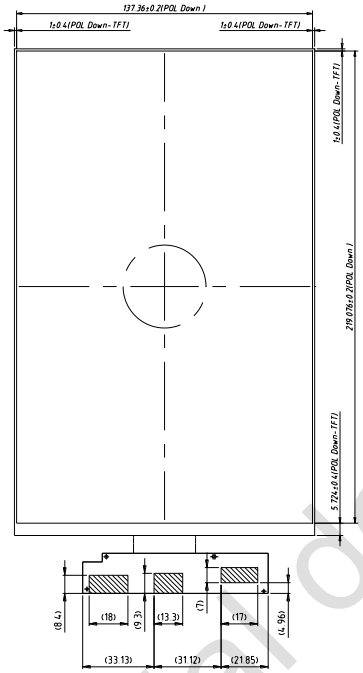
5.1 Outline Drawing

Figure 20 Reference Outline Drawing (Front Side)



Unit:mm

Figure 21 Reference Outline Drawing (Back Side)



Unit:mm

Note: Unnoted tolerance ±0.5mm;

5.2 Dimension Specifications

Table 23 Open-cell Dimension Specifications

Item	Min.	Typ.	Max.	Unit
Width	(139.16)	(139.36)	(139.56)	mm
Height (Without PCBA)	(225.6)	(225.8)	(226.0)	mm
Height (With PCBA)	(251.658)	(252.658)	(253.658)	mm
Thickness	-	-	(1.75)	mm
Weight	-	-	(85)	g

Note：Outline dimension measure instrument: Vernier Caliper.

6.0 Reliability Conditions

Table 24 Reliability Condition

Item	Package	Test Conditions	Note
High Temperature/High Humidity Operating Test	Open-cell	T_{gs}=40℃, 90%RH, 300 hours	(1),(2), (3),(4)
High Temperature Operating Test	Open-cell	T_{gs}=50℃, 300 hours	
Low Temperature Operating Test	Open-cell	T_a=0℃, 300 hours	
High Temperature Storage Test	Open-cell	T_a=60℃, 300 hours	
Low Temperature Storage Test	Open-cell	T_a= -20℃, 300 hours	

Note (1) A sample can only have one test. Outward appearance, image quality and optical data can only be checked at normal conditions according to the IVO document before reliable test. Only check the function of the open-cell after reliability test.

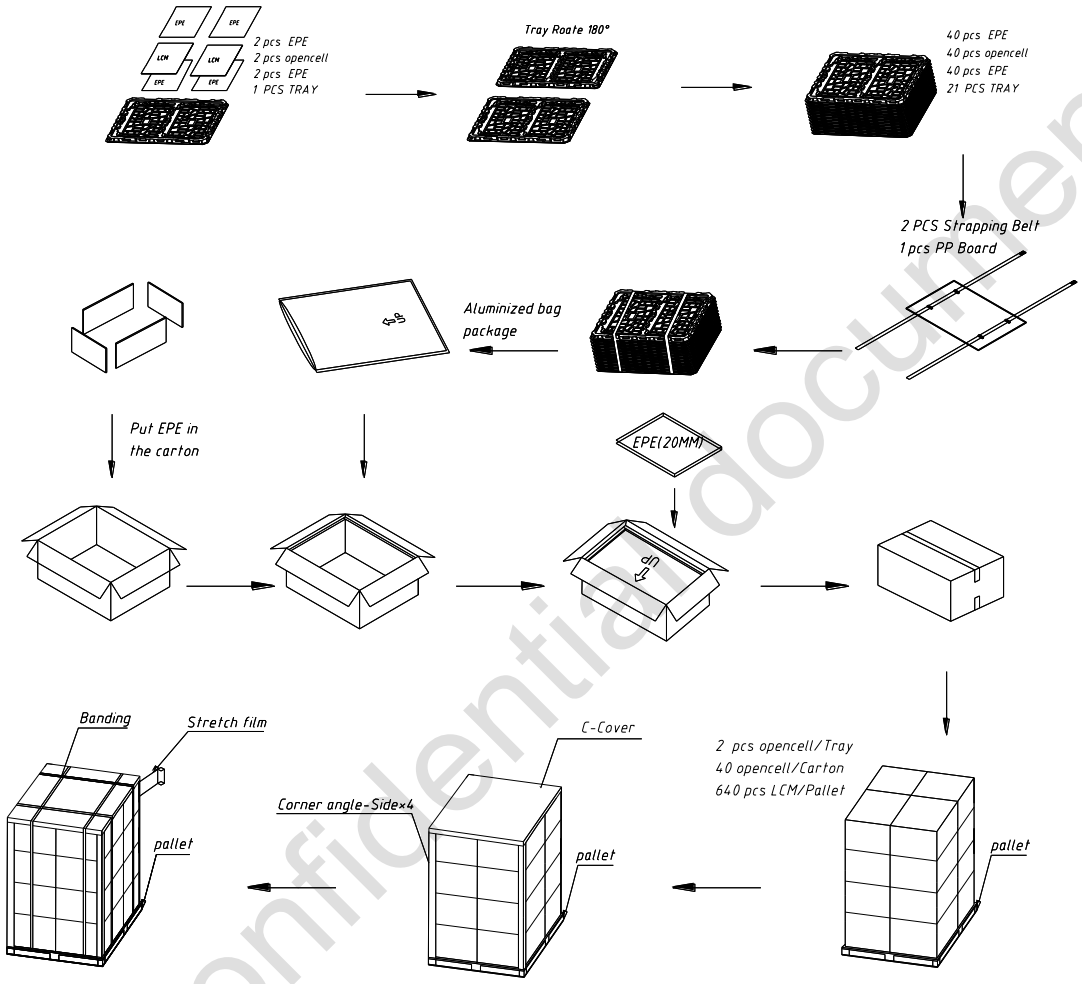
Note (2) The setting of electrical parameters should follow the typical value before reliability test.

Note (3) During the test, it is unaccepted to have condensate water remains. Besides, protect the open-cell from static electricity.

Note (4) The sample must be released for 24 hours under normal conditions before judging. Furthermore, all the judgment must be made under normal conditions. Normal conditions are defined as follow: Temperature: 25℃, Humidity: 55± 10%RH. T_a= Ambient Temperature, T_{gs}= Glass Surface Temperature.

7.0 Package Specification

Figure 23 Packing Method



8.0 Lot Mark

TBD

9.0 General Precaution

9.1 Using Restriction

This product is not authorized for using in life supporting systems, aircraft navigation control systems, military systems and any other appliance where performance failure could be life-threatening or lead to be catastrophic.

9.2 Operation Precaution

(1)The LCD product should be operated under normal conditions.
Normal conditions are defined as below:

Temperature: 25℃

Humidity: 55±10%

Display pattern: continually changing pattern (Not stationary)

(2) Brightness and response time depend on the temperature. (It needs more time to reach normal brightness in low temperature.)

(3) It is necessary for you to pay attention to condensation when the ambient temperature drops suddenly. Condensate water would damage the polarizer and electrical contacted parts of the open-cell. Besides, smear or spot will remain after condensate water evaporating.

(4) If the absolute maximum rating value was exceeded, it may damage the open-cell.

(5) Do not adjust the variable resistor located on the open-cell.

(6) Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding may be important to minimize the interference.

(7) Image sticking may occur when the panel displayed the same pattern for long time.

(8) Do not connect or disconnect the open-cell in the “power on” condition. Power supply should always be turned on/off by the “power on/off sequence”

(9) Ultra-violet ray filter is necessary for outdoor operation.

9.3 Mounting Precaution

(1) All the operators should be electrically grounded and with Ion-blown equipment turning on when mounting or handling. Dressing finger-stalls out of the gloves is important for keeping the panel clean during the incoming inspection and the process of assembly.

(2) It is unacceptable that the material of cover case contains acetic or chloric. Besides, any other material that could generate corrosive gas or cause circuit break by electro-chemical reaction is not desirable.

(3) Do not damage the PCBA. And it is recommended to use packing trays while carrying

(4) The mounting structure should be taken into consideration so that uneven force (ex. Twisted stress) is not applied to the open-cell. The case on which an open-cell is mounted should have sufficient strength so that external force is not transmitted to the open-cell directly.

(5) It is obvious that you should adopt radiation structure to satisfy the temperature specification.

(6) So as to acquire higher luminance, the cable of the power supply should be connected directly with a minimize length.
(7) A transparent protective film needs to be attached to the surface of the open-cell.
(8) Do not press or scratch the polarizer exposed with anything harder than HB pencil lead. In addition, don't touch the pin exposed with bare hands directly.
(9) Clean the polarizer gently with absorbent cotton or soft cloth when it is dirty.
(10) Wipe off saliva or water droplet as soon as possible. Otherwise, it may cause deformation and fading of color.
(11) Desirable cleaners are IPA (Isopropyl Alcohol) or hexane. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(12) Do not disassemble or modify the open-cell. It may damage sensitive parts in the LCD open-cell, and cause scratches or dust remains. IVO does not warrant the open-cell, if you disassemble or modify the open-cell.

9.4 Handling Precaution

(1) Static electricity will generate between the film and polarizer, when the protection film is peeled off. It should be peeled off slowly and carefully by operators who are electrically grounded and with Ion-blown equipment turning on. Besides, it is recommended to peel off the film from the bonding area.
(2) The protection film is attached to the polarizer with a small amount of glue. When the open-cell with protection film attached is stored for a long time, a little glue may remain after peeling.
(3) If the liquid crystal material leaks from the panel, keep it away from the eyes and mouth. In case of contact with hands, legs or clothes, it must be clean with soap thoroughly.

9.5 Storage Precaution

When storing the open-cell as spares for long time, the following precautions must be executed.
(1) Store them in a dark place. Do not expose to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.
(2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.
(3) It is recommended to use it in a short-time period, after it's unpacked. Otherwise, we would not guarantee the quality.

9.6 Others

When disposing LCD open-cell, obey the local environmental regulations.