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Document No.	A-E102AWF2-R6-468-02	Issue date	2021/04/15	Revision	00

Customer Approved Specification

To: 苏州与来视讯科技有限公司

Product Name: E102AWF2 R6

Document Issue Date: 2021/04/15

Customer	InfoVision Optoelectronics
SIGNATURE Please return 1 copy for your confirmation with your signature and comments.	**SIGNATURE** **REVIEWED BY CQM** **PREPARED BY FAE**

Note : 1. Please contact InfoVision Company before designing your product based on this product.
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by IVO for any intellectual property claims or other problems that may result from application based on the module described herein.

FQ-7-30-0-009-03D

Revision	Date	Page	Revised Content/Summary	Remark
00	2021/04/15	--	First issued.	

CONTENTS

1.0 General Descriptions

1.1 Introduction

The E102AWF2 R6 is a Color Active Matrix Liquid Crystal Display. The matrix uses a-Si Thin Film Transistor as a switching device. This TFT LCD has a 10.25 inch diagonally measured active display area with FHD resolution (1,920 horizontal by 720 vertical pixels array).

1.2 Features

- Supported FHD Resolution
- LVDS Interface
- Wide View Angle
- Compatible with RoHS Standard

1.3 Product Summary

Items	Specifications	Unit
Screen Diagonal	10.25	inch
Active Area (H x V)	243.648 x 91.368	mm
Number of Pixels (H x V)	1,920 x 720	-
Pixel Pitch (H x V)	0.1269 x 0.1269	mm
Pixel Arrangement	R.G.B. Vertical Stripe	-
Display Mode	Normally Black	-
Contrast Ratio	(900) (Typ.)	-
Response Time	(20)(Typ.)	ms
Input Voltage	(3.3) (Typ.)	V
Weight	(95) (Max.)	g
Outline Dimension (H x V x D)	(252.2) (Typ.) x (103.2)(Typ.) x (1.426)(Max.)	mm
Electrical Interface (Logic)	LVDS	-
Support Color	16.7 M (8bit)	-
NTSC	(68) (Typ.)	%
Surface Treatment	HC	-
Transmittance	(3.6)(Typ.)	%

1.4 Functional Block Diagram

Figure 1 shows the functional block diagram of the LCD module.

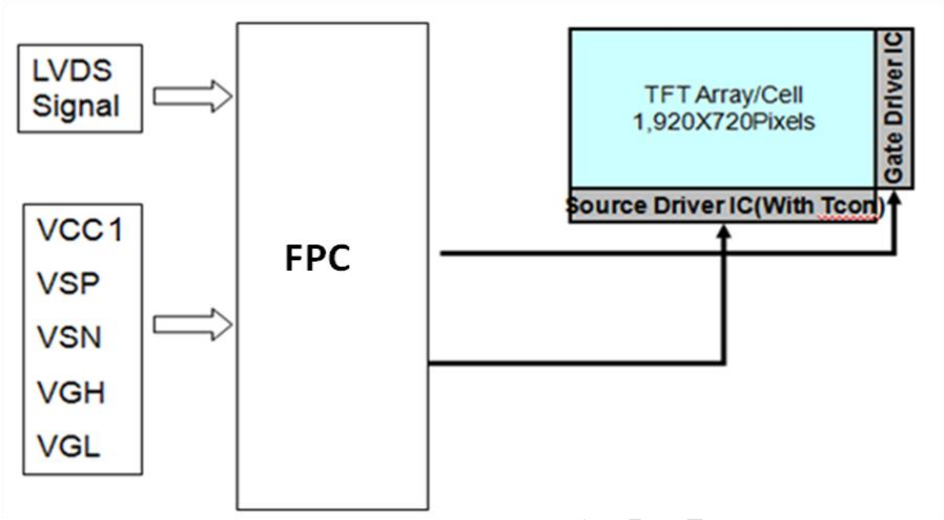

Figure 1 Block Diagram

1.5 Pixel Mapping

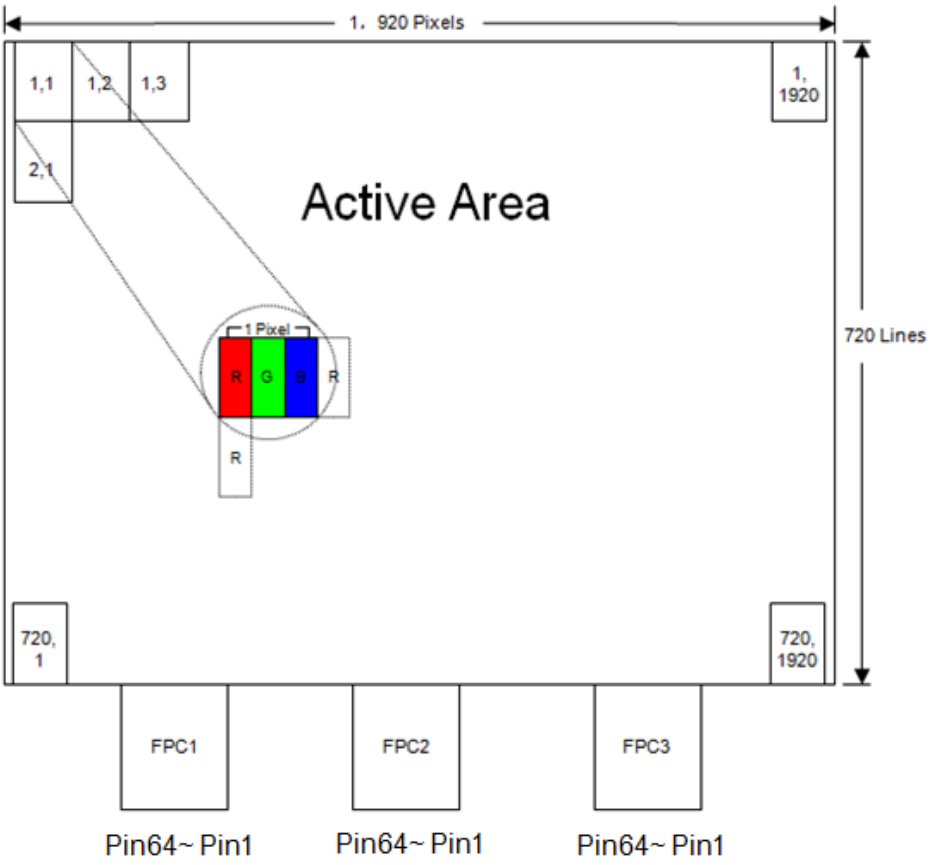

Figure 2 Pixel Mapping

2.0 Absolute Maximum Ratings

Table 1 Electrical & Environment Absolute Rating

Item	Symbol	Min.	Max.	Unit	Note
Power supply voltage	VCC1	(-0.3)	(4)	V	GND=0 (1),(2), (3),(4)
	VSP	(-0.3)	(7.7)	V	
	VSN	(-7.7)	(-0.5)	V	
	VGH	(-0.3)	(VGL+42)	V	
	VGL	(-25)	(0.3)	V	
Programming voltage	VDD_OTP	(-0.3)	(8.75)	V	
Digital I/O input signals	V_{IO}	(-0.3)	(VCC1+0.3)	V	
Operating Temperature	T_{gs}	-20	70	℃	(1),(2), (3),(4)
Storage Temperature	T_a	-30	85	℃	

Note (1) All the parameters specified in the table are absolute maximum rating values that may cause faulty operation or unrecoverable damage, if exceeded. It is recommended to follow the typical value.

Note (2) All the contents of electro-optical specifications and display fineness are guaranteed under Normal Conditions. All the display fineness should be inspected under normal conditions. Normal conditions are defined as follow: Temperature: 25℃, Humidity: 55± 10%RH.

Note (3) Unpredictable results may occur when it was used in extreme conditions. T_a= Ambient Temperature, T_{gs}= Glass Surface Temperature. All the display fineness should be inspected under normal conditions.

Note (4) Temperature and relative humidity range are shown in the figure below. Wet bulb temperature should be lower than 57.8℃, and no condensation of water. Besides, protect the module from static electricity.

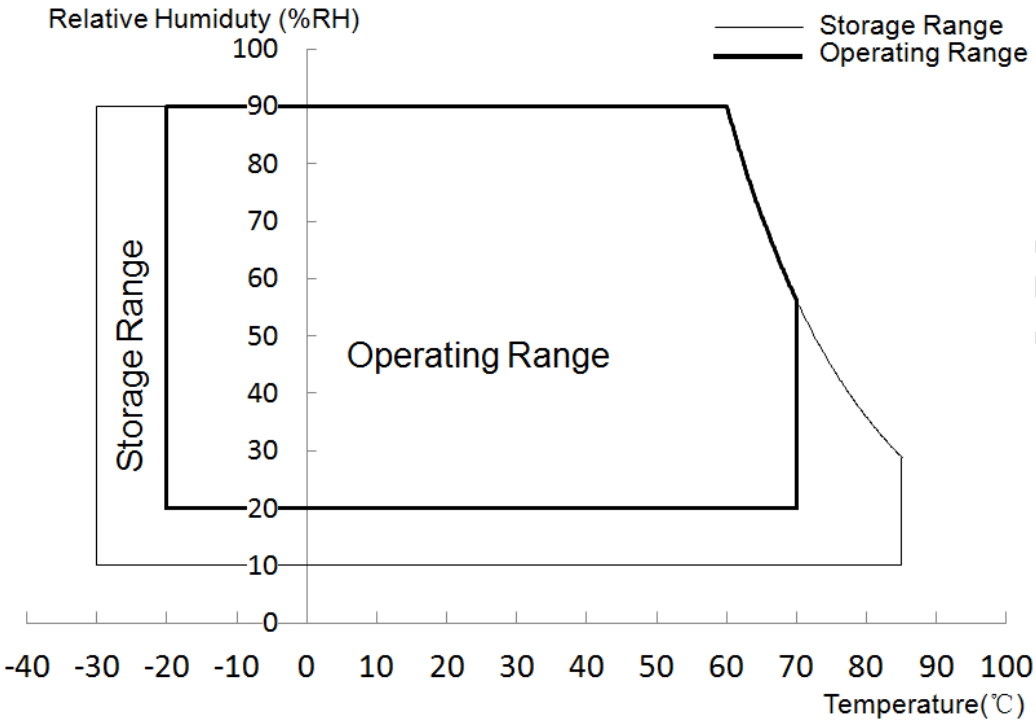

Figure 3 Absolute Ratings of Environment of the LCD Module

3.0 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes.

Table 2 Optical Characteristics

Item	Conditions		Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR≥10)	Horizontal	θ_{x+}	(80)	(85)	-	degree	(1),(2),(3),(6),(7)
		θ_{x-}	(80)	(85)	-		
	Vertical	θ_{y+}	(80)	(85)	-		
		θ_{y-}	(80)	(85)	-		
Contrast Ratio	Center		(700)	(900)	-	-	(1),(3),(6),(7) θx=θy=0°
Response Time	Rising + Falling @25℃		-	(20)	(30)	ms	(1),(4),(6),(7) θx=θy=0°
Transmittance	-		(3.2)	(3.6)	-	%	(1),(5),(7) θx=θy=0° (Under C-light)
Color Chromaticity (CIE1931)	Red	x	Typ. (-0.02)	(0.657)	Typ. (+0.02)	-	(1),(5),(7) θx=θy=0° (Under C-light)
	Red	y		(0.326)		-	
	Green	x		(0.289)		-	
	Green	y		(0.608)		-	
	Blue	x		(0.132)		-	
	Blue	y		(0.143)		-	
	White	x		(0.325)		-	
	White	y		(0.376)		-	
NTSC	-		65	(68)	-	%	

Note (1) Measurement Setup:

The LCD module should be stabilized at given ambient temperature (25℃) for 30 minutes to avoid abrupt temperature changing during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 30 minutes in the windless room.

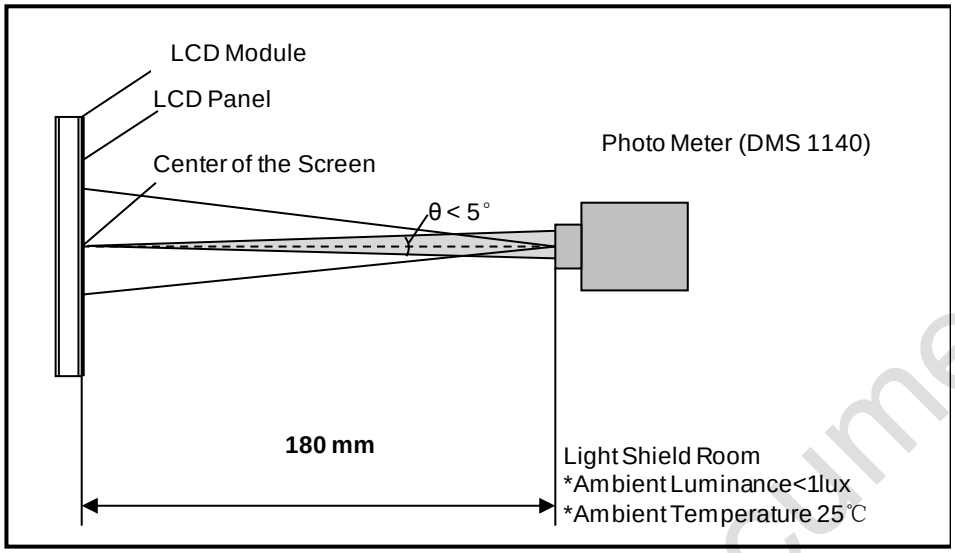

Figure 4 Measurement Setup

Note (2) Definition of Viewing Angle

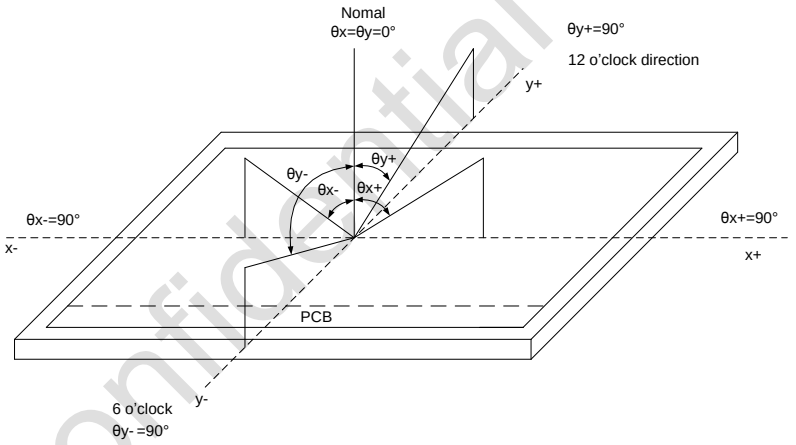

Figure 5 Definition of Viewing Angle

Note (3) Definition of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression:

Contrast Ratio (CR) = The luminance of White pattern/ The luminance of Black pattern

Note (4) Definition of Response Time (T_R, T_F)

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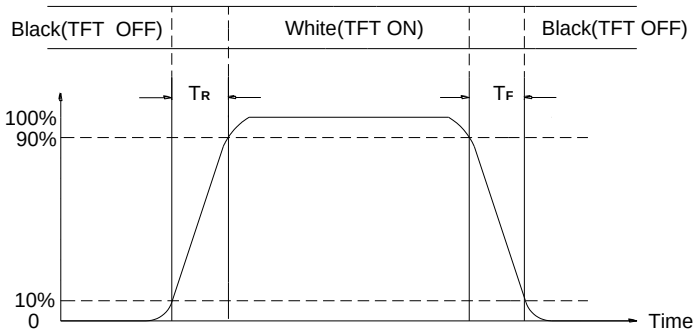


Figure 6 Definition of Response Time

Note (5) C-Light Spectrum

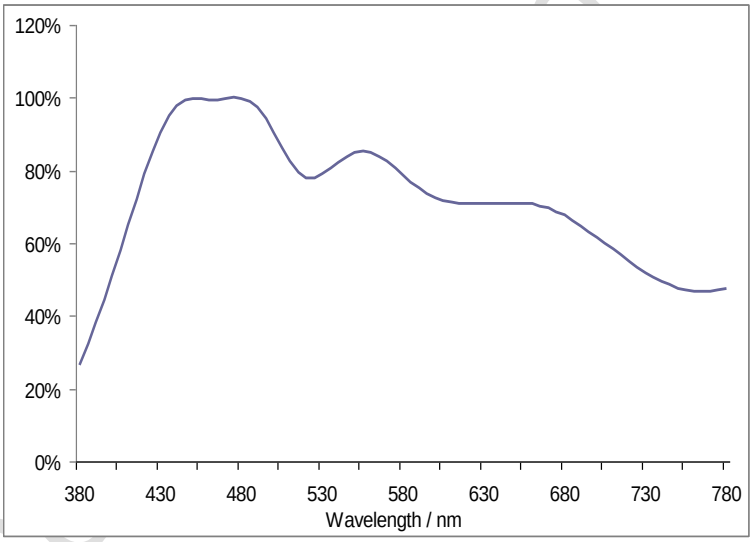


Figure 7 C-Light Spectrum

Note (6) Light source is the BL which is supplied by Customer.

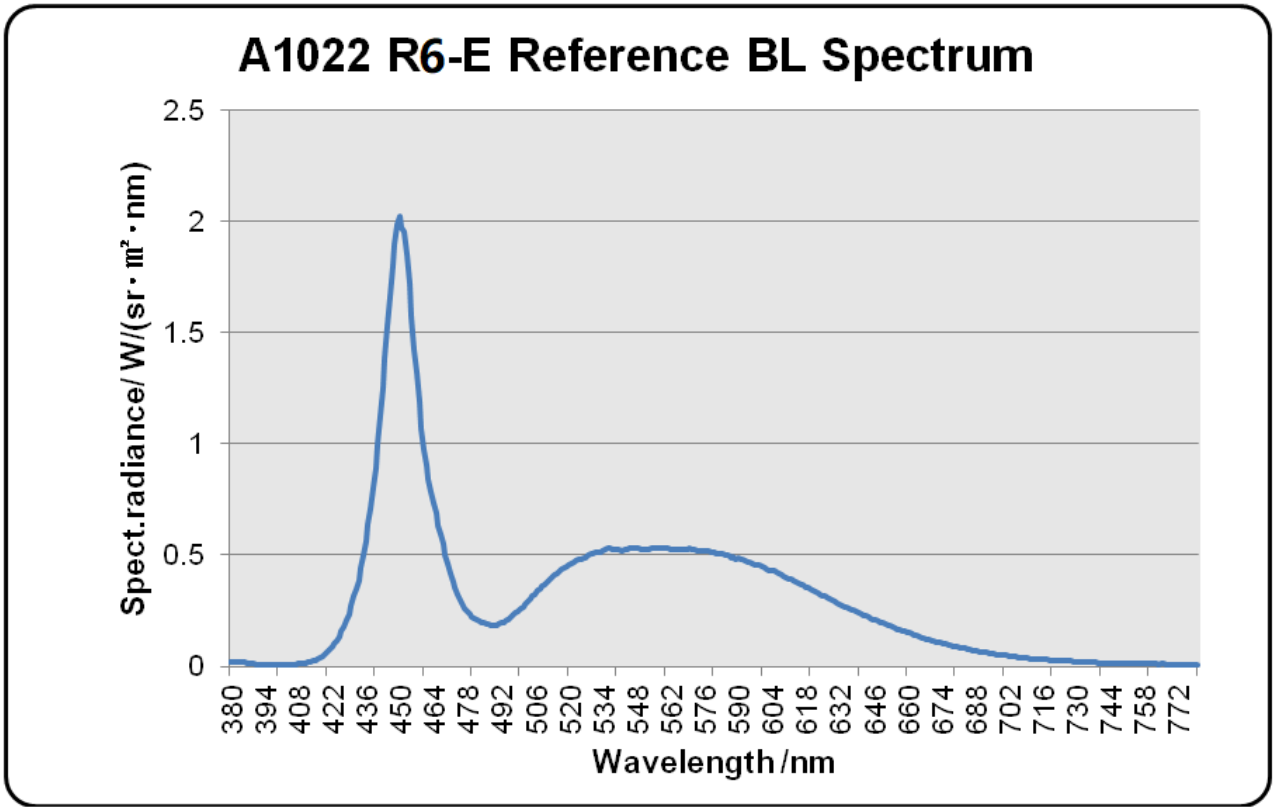


Figure 8 Back Light Spectrum

Note (7) All optical data are based on IVO given system & nominal parameter & testing machine in this document.

4.0 Electrical Characteristics

4.1 Interface Connector

Table 3 Signal Connector Type

Item	Description
Mating Receptacle / Type (Reference)	AORORA F31L-1A7H1-11064-E120 or Compatible

Table 4 Signal FPC1 Pin Assignment

Pin No.	Symbol	Function	Remarks
1	NC	No connection	-
2	NC	No connection	-
3	ATREN	Enable auto reload OTP every 60 frames (Short to FPC2's and FPC3's ATREN when PCBA design. And when OTP programming, ATREN pull L.) ATREN=H:Enable auto reload OTP(Default) ATREN=L:Disable auto reload OTP	-
4	NC	No connection	-
5	NC	No connection	-
6	NC	No connection	-
7	NC	No connection	-
8	NC	No connection	-
9	VCOM	Power input for LCD common electrode (Require a 2.2uF and 0.1uF capacitor to GND as close to FPC1's VCOM as possible, and short to FPC2's and FPC3's VCOM when PCBA design.)	-
10	VCL1	Internal regulator output for negative level shifter (-3V)(Require a 2.2uF capacitor to GND as close to FPC1's VCL1 as possible.)	-
11	VSN	Power input for source driver and power circuits (Require a 4.7uF and 0.1uF capacitor and 10KΩ resistance to GND as close to FPC1's VSN as possible and Short to FPC2's and FPC3's VSN when PCBA design.)	-
12	GND	GND	-
13	VSP	Power input for source driver and power circuits (Require a 4.7uF and 0.1uF capacitor and 10KΩ resistance to GND as close to FPC1's VSP as possible and Short to FPC2's and FPC3's VSP when PCBA design.)	-

14	INV0	Inversion type selection. H：Dot Inversion L：1+2Dot Inversion Short to FPC2's and FPC3's INV0 when PCBA design. (IVO suggestion: Please pull L on PCBA)	-
15	I2C_SCL	Serial Interface clock input (Please Pull H with 4.7KΩ resistance and short to FPC2's and FPC3's I2C_SCL when PCBA design.)	-
16	I2C_SDA	Serial Interface address and data (Please Pull H with 4.7KΩ resistance and short to FPC2's and FPC3's I2C_SDA when PCBA design.)	-
17	RESETB	Global Reset pin. Active low(RESETB must meet the sequence of Driver IC when power on/off ;Add external RC circuit(R=10KΩ,C= 1uF) to pin RESETB to start whole chip reset when power up and short to FPC2's and FPC3's RESETB when PCBA design.)	-
18	STBYB	Standby mode setting pin. Active low. Timing controller, output buffer, DAC and power circuit all off when STBYB is low.(Add external RC circuit(R=10KΩ,C= 1uF) to pin STBYB to start whole chip STBYB when power up .STBYB must meet the sequence of Driver IC when power on/off; And short to FPC2's and FPC3's STBYB when PCBA design.)	-
19	VCC1	Power input for main and I/O power (Require a 4.7uF and 0.1uF capacitor to GND as close to FPC1's VCC1 as possible and short to FPC2's and FPC3's VCC1 when PCBA design.)	-
20	VDDD1	Internal regulator output for logic power supply (3.3V) (Require a 2.2uF capacitor to GND as close to FPC1's VDDD as possible when PCBA design.)	-
21	VDDDIF1	Internal regulator output for interface power supply (3.3V) (Require a 2.2uF capacitor to GND as close to FPC1's VDDDIF as possible when PCBA design.)	-
22	GND	GND	-
23	ELV3P	LVDS data lane 3 Positive	-
24	ELV3N	LVDS data lane 3 Negative	-
25	GND	GND	

26	ELV2P	LVDS data lane 2 Positive	-
27	ELV2N	LVDS data lane 2 Negative	-
28	GND	GND	-
29	ELVCLKP	LVDS Clock Lane Positive	-
30	ELVCLKN	LVDS Clock Lane Negative	
31	GND	GND	-
32	ELV1P	LVDS Data Lane 1 Positive	-
33	ELV1N	LVDS Data Lane 1 Negative	-
34	GND	GND	-
35	ELV0P	LVDS Data Lane 0 Positive	
36	ELV0N	LVDS Data Lane 0 Negative	-
37	GND	GND	-
38	OLV3P	LVDS data lane 3 Positive	-
39	OLV3N	LVDS data lane 3 Negative	-
40	GND	GND	-
41	OLV2P	LVDS data lane 2 Positive	-
42	OLV2N	LVDS data lane 2 Negative	-
43	GND	GND	-
44	OLVCLKP	LVDS Clock Lane Positive	-
45	OLVCLKN	LVDS Clock Lane Negative	-
46	GND	GND	
47	OLV1P	LVDS Data Lane 1 Positive	-
48	OLV1N	LVDS Data Lane 1 Negative	-
49	GND	GND	-
50	OLV0P	LVDS Data Lane 0 Positive	-
51	OLV0N	LVDS Data Lane 0 Negative	-
52	GND	GND	-
53	VGMPHO	Internal regulator output for positive gamma reference voltage (Require a 2.2uF capacitor to GND as close to FPC1's VGMPHO as possible and short to FPC2's and FPC3's VGMPHI when PCBA design.)	-
54	VGMPMO	Internal regulator output for positive gamma reference voltage (Require a 2.2uF capacitor to GND as close to FPC1's VGMPMO as possible and short to FPC2's and FPC3's	-

		VGMPMI when PCBA design.)	
55	VGMPLO	Internal regulator output for positive gamma reference voltage (Require a 2.2uF capacitor to GND as close to FPC1's VGMPLO as possible and short to FPC2's and FPC3's VGMPLI when PCBA design.)	-
56	VGMNHO	Internal regulator output for negative gamma reference voltage (Require a 2.2uF capacitor to GND as close to FPC1's VGMNHO as possible and short to FPC2's and FPC3's VGMNHI when PCBA design.)	-
57	VGMNMO	Internal regulator output for negative gamma reference voltage (Require a 2.2uF capacitor to GND as close to FPC1's VGMNMO as possible and short to FPC2's and FPC3's VGMNMI when PCBA design.)	-
58	VGMNLO	Internal regulator output for negative gamma reference voltage (Require a 2.2uF capacitor to GND as close to FPC1's VGMNLO as possible and short to FPC2's and FPC3's VGMNLI when PCBA design.)	-
59	FAIL_DET1	Fail detection signal output (Please short to FPC2's and FPC3's FAIL_DET when PCBA design.)	-
60	FCS	Function detection by Hardware/Software selection FCS=H: Hardware pin FCS=L: Software register Short to FPC2's and FPC3's FCS when PCBA design. (IVO suggestion: Please pull H on PCBA)	-
61	RL	Horizontal shift direction RL=H: Forward(SOUT1→ SOUT2→...→SOUT1920) RL=L: Reverse(SOUT1920→SOUT1919→...→S1) Short to FPC2's and FPC3's RL when PCBA design	-
62	TB	Vertical shift direction(gate output) selection TB=H: Forward, Top → Bottom TB=L: Reverse, Bottom → Top Short to FPC2's and FPC3's TB when PCBA design.	-
63	BISTEN	Enable built-in self test (BIST) function BISTEN=H: BIST mode BISTEN=L: Normal mode	-

		(Not use, please leave it to GND) Short to FPC2's and FPC3' BISTEN when PCBA design.	
64	VDD_OTP	Power input for OTP programming (8.5V). Leave this pin open or connect it to VCC1 when not programming OTP (Require a 2.2uF capacitor to GND as close to FPC1's VDD_OTP as possible and Short to FPC2's and FPC3's VDD_OTP when PCBA design.)	-

Table 5 Signal FPC2 Pin Assignment

Pin No.	Symbol	Function	Remarks
1	NC	No connection	-
2	NC	No connection	-
3	ATREN	Enable auto reload OTP every 60 frames ATREN=H:Enable auto reload OTP(Default) ATREN=L:Disable auto reload OTP	-
4	NC	No connection	-
5	NC	No connection	-
6	NC	No connection	-
7	NC	No connection	-
8	NC	No connection	-
9	VCOM	Power input for LCD common electrode (Require a 2.2uF and 0.1uF capacitor to GND as close to FPC2's VCOM as possible.)	-
10	VCL2	Internal regulator output for negative level shifter (-3V)(Require a 2.2uF capacitor to GND as close to FPC2's VCL2 as possible.)	-
11	VSN	Power input for source driver and power circuits (Require a 4.7uF and 0.1uF capacitor to GND as close to FPC2's VSN as possible.)	-
12	GND	GND	-
13	VSP	Power input for source driver and power circuits (Require a 4.7uF and 0.1uF capacitor to GND as close to FPC2's VSP as possible.)	-

14	INV0	Inversion type selection. H：Dot Inversion L：1+2Dot Inversion	-
15	I2C_SCL	Serial Interface clock input	-
16	I2C_SDA	Serial Interface address and data	-
17	RESETB	Global Reset pin. Active low	-
18	STBYB	Standby mode setting pin. Active low. Timing controller, output buffer, DAC and power circuit all off when STBYB is low.	-
19	VCC1	Power input for main and I/O power (Require a 4.7uF and 0.1uF capacitance to GND as close to FPC2's VCC1 as possible.)	-
20	VDDD2	Internal regulator output for logic power supply (3.3V) (Require a 2.2uF capacitor to GND when PCBA design.)	-
21	VDDDIF2	Internal regulator output for interface power supply (3.3V) (Require a 2.2uF capacitor to GND when PCBA design.)	-
22	GND	GND	-
23	ELV3P	LVDS data lane 3 Positive	-
24	ELV3N	LVDS data lane 3 Negative	-
25	GND	GND	
26	ELV2P	LVDS data lane 2 Positive	-
27	ELV2N	LVDS data lane 2 Negative	-
28	GND	GND	-
29	ELVCLKP	LVDS Clock Lane Positive	-
30	ELVCLKN	LVDS Clock Lane Negative	
31	GND	GND	-
32	ELV1P	LVDS Data Lane 1 Positive	-
33	ELV1N	LVDS Data Lane 1 Negative	-
34	GND	GND	-
35	ELV0P	LVDS Data Lane 0 Positive	
36	ELV0N	LVDS Data Lane 0 Negative	-

37	GND	GND	-
38	OLV3P	LVDS data lane 3 Positive	-
39	OLV3N	LVDS data lane 3 Negative	-
40	GND	GND	-
41	OLV2P	LVDS data lane 2 Positive	-
42	OLV2N	LVDS data lane 2 Negative	-
43	GND	GND	-
44	OLVCLKP	LVDS Clock Lane Positive	-
45	OLVCLKN	LVDS Clock Lane Negative	-
46	GND	GND	
47	OLV1P	LVDS Data Lane 1 Positive	-
48	OLV1N	LVDS Data Lane 1 Negative	-
49	GND	GND	-
50	OLV0P	LVDS Data Lane 0 Positive	-
51	OLV0N	LVDS Data Lane 0 Negative	-
52	GND	GND	-
53	VGMPHI	Positive gamma reference voltage (From FPC1's VGMPHO)	-
54	VGMPMI	Positive gamma reference voltage (From FPC1's VGMPMO)	-
55	VGMPLI	Positive gamma reference voltage (From FPC1's VGMPLO)	-
56	VGMNHI	Negative gamma reference voltage (From FPC1's VGMNHO)	-
57	VGMNMI	Negative gamma reference voltage (From FPC1's VGMNMO)	-
58	VGMNLI	Negative gamma reference voltage (From FPC1's VGMNLO)	-
59	FAIL_DET2	Fail detection signal output(Please reserve a test point when PCBA design.)	-
60	FCS	Function detection by Hardware/Software selection FCS=H: Hardware pin FCS=L: Software register	-

61	RL	Horizontal shift direction RL=H: Forward(SOUT1→ SOUT2→...→SOUT1920) RL=L: Reverse(SOUT1920→SOUT1919→...→S1)	-
62	TB	Vertical shift direction(gate output) selection TB=H: Forward, Top → Bottom TB=L: Reverse, Bottom → Top	-
63	BISTEN	Enable built-in self test (BIST) function BISTEN=H: BIST mode BISTEN=L: Normal mode (Not use, please leave it to GND)	-
64	VDD_OTP	Power input for OTP programming (8.6V). Leave this pin open or connect it to VCC1 when not programming OTP (Require a 2.2uF capacitor to GND as close to FPC2's VDD_OTP as possible.)	-

Table 6 Signal FPC3 Pin Assignment

Pin No.	Symbol	Function	Remarks
1	SGOFF2	The SGOFF1/ SGOFF2 signal control the slow gate off function. When they are not used, connecting to GND is recommended.(IVO suggestion: short to GND on PCBA)	-
2	SGOFF1		-
3	ATREN	Enable auto reload OTP every 60 frames ATREN=H:Enable auto reload OTP(Default) ATREN=L:Disable auto reload OTP	-
4	VGN	Slow gate off function control pin. When slow gate off is disabled, connecting VGN to VDD is forbidden, connecting VGN to GND, VGL or VGH, or keeping it floating is recommended. (IVO suggestion: keep it floating on PCBA)	-
5	VGL	Power supply for analog power (Require a 2.2uF and 0.1uF capacitor and 10KΩ resistance and Schottky diode to GND as close to FPC3' VGL as possible when PCBA design.)	-
6	NC	No connection	-
7	VGH	Power supply for analog power (Require a 2.2uF and 0.1uF capacitor to GND as close to FPC3's VGH as possible when PCBA design.)	-
8	NC	No connection	-
9	VCOM	Power input for LCD common electrode (Require a 2.2uF and 0.1uF capacitor to GND as close to FPC3's VCOM as possible.)	-
10	VCL3	Internal regulator output for negative level shifter (-3V) (Require a 2.2uF capacitor to GND as close to FPC3's VCL3 as possible.)	-
11	VSN	Power input for source driver and power circuits (Require a 4.7uF and 0.1uF capacitor to GND as close to FPC3's VSN as possible.)	-
12	GND	GND	-
13	VSP	Power input for source driver and power circuits (Require a 4.7uF and 0.1uF capacitor to GND as close to FPC3's VSP as possible.)	-
14	INV0	Inversion type selection. H：Dot Inversion L：1+2Dot Inversion	-
15	I2C_SCL	Serial Interface clock input	-
16	I2C_SDA	Serial Interface address and data	-
17	RESETB	Global Reset pin. Active low	-
18	STBYB	Standby mode setting pin. Active low. Timing controller, output buffer,	-

		DAC and power circuit all off when STBYB is low.	
19	VCC1	Power input for main and I/O power (Require a 4.7uF and 0.1uF capacitance to GND as close to FPC3's VCC1 as possible)	-
20	VDDD3	Internal regulator output for logic power supply (3.3V) (Require a 2.2uF capacitor to GND when PCBA design.)	-
21	VDDDIF3	Internal regulator output for interface power supply (3.3V) (Require a 2.2uF capacitor to GND when PCBA design.)	-
22	GND	GND	-
23	ELV3P	LVDS data lane 3 Positive	-
24	ELV3N	LVDS data lane 3 Negative	-
25	GND	GND	-
26	ELV2P	LVDS data lane 2 Positive	-
27	ELV2N	LVDS data lane 2 Negative	-
28	GND	GND	-
29	ELVCLKP	LVDS Clock Lane Positive	-
30	ELVCLKN	LVDS Clock Lane Negative	-
31	GND	GND	-
32	ELV1P	LVDS Data Lane 1 Positive	-
33	ELV1N	LVDS Data Lane 1 Negative	-
34	GND	GND	-
35	ELV0P	LVDS Data Lane 0 Positive	-
36	ELV0N	LVDS Data Lane 0 Negative	-
37	GND	GND	-
38	OLV3P	LVDS data lane 3 Positive	-
39	OLV3N	LVDS data lane 3 Negative	-
40	GND	GND	-
41	OLV2P	LVDS data lane 2 Positive	-
42	OLV2N	LVDS data lane 2 Negative	-
43	GND	GND	-
44	OLVCLKP	LVDS Clock Lane Positive	-
45	OLVCLKN	LVDS Clock Lane Negative	-
46	GND	GND	-
47	OLV1P	LVDS Data Lane 1 Positive	-
48	OLV1N	LVDS Data Lane 1 Negative	-

49	GND	GND	-
50	OLV0P	LVDS Data Lane 0 Positive	-
51	OLV0N	LVDS Data Lane 0 Negative	-
52	GND	GND	-
53	VGMPHI	Positive gamma reference voltage (From FPC1's VGMPHO)	-
54	VGMPMI	Positive gamma reference voltage (From FPC1's VGMPMO)	-
55	VGMPLI	Positive gamma reference voltage (From FPC1's VGMPLO)	-
56	VGMNHI	Negative gamma reference voltage (From FPC1's VGMNHO)	-
57	VGMNMI	Negative gamma reference voltage (From FPC1's VGMNMO)	-
58	VGMNLI	Negative gamma reference voltage (From FPC1's VGMNLO)	-
59	FAIL_DET3	Fail detection signal output (Please reserve a test point when PCBA design.)	-
60	FCS	Function detection by Hardware/Software selection FCS=H: Hardware pin FCS=L: Software register	-
61	RL	Horizontal shift direction RL=H: Forward(SOUT1→ SOUT2→...→SOUT1920) RL=L: Reverse(SOUT1920→SOUT1919→...→S1)	Note1
62	TB	Vertical shift direction(gate output) selection TB=H: Forward, Top → Bottom TB=L: Reverse, Bottom → Top	Note1
63	BISTEN	Enable built-in self test (BIST) function BISTEN=H: BIST mode BISTEN=L: Normal mode (Not use, please leave it to GND)	-
64	VDD_OTP	Power input for OTP programming (8.5V). Leave this pin open or connect it to VCC1 when not programming OTP (Require a 2.2uF capacitor to GND as close to FPC3's VDD_OTP as possible.)	-

Note：TB and RL control function

RL	TB	Scan direction
H	H	Data scan from left to right; Gate scan from up to down
L	H	Data scan from right to left; Gate scan from up to down
H	L	Data scan from left to right; Gate scan from down to up
L	L	Data scan from right to left; Gate scan from down to up

4.1.1 FPC Cascade Design for Customer

4.1.1.1The Reference Design of External Power on PCBA is as Follows:

（1）The VGH/VGL voltages are provided by external power (Figure 9)；

（2）The capacitors of VGH/VGL need to be as close to FPC as possible(Figure 9)；

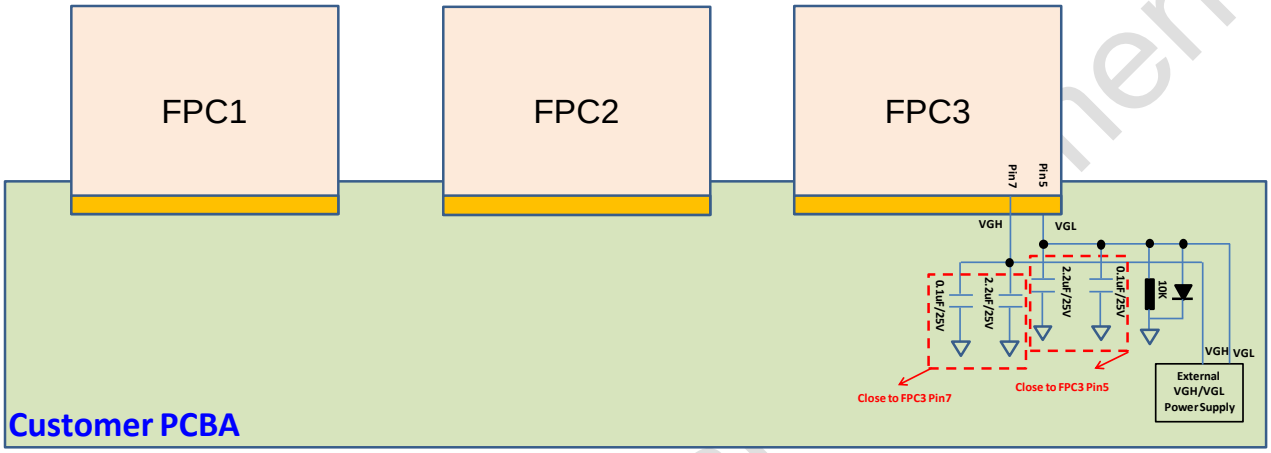


Figure 9: Cascade design with external Power Supply (VGH/VGL)

（3）The VSP/VSN voltages are provided by external power (Figure 10)；

（4）The capacitors of VSP/VSN need to be as close to FPC1 as possible (Figure 10)；

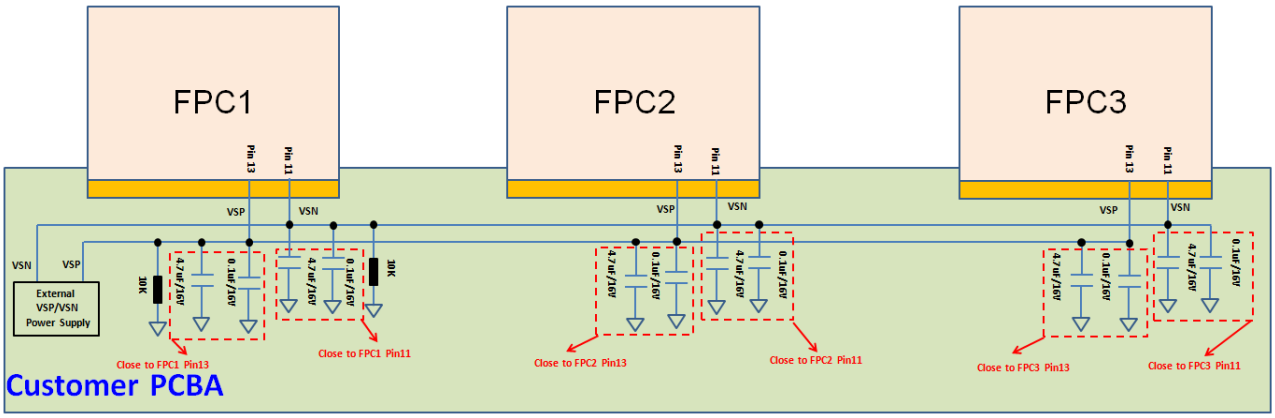


Figure 10: Cascade design with external Power Supply(VSP/VSN)

（5）The VCC1 voltages are provided by external power (Figure 11) ；

（6）The capacitors of VCC1 need to be as close to FPC as possible (Figure 11)；

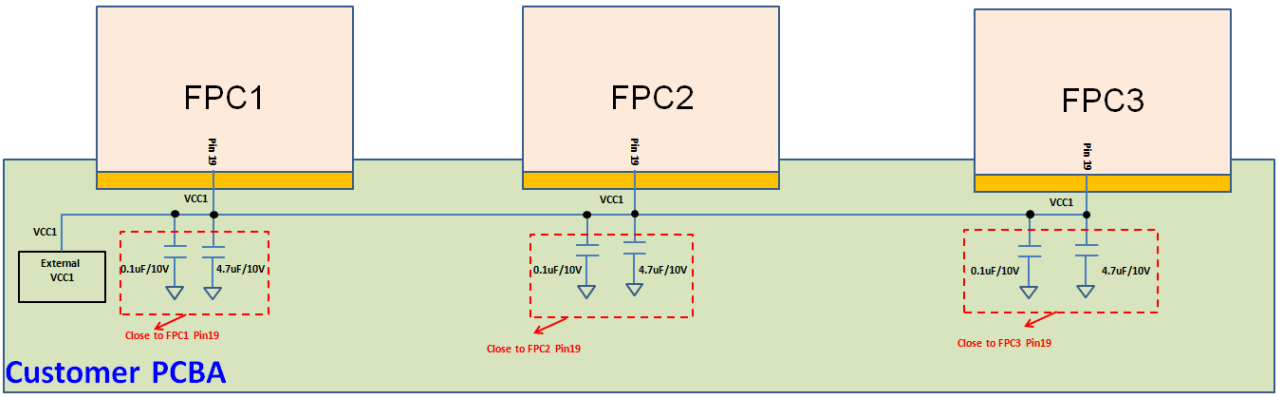


Figure 11: Cascade design with external Power Supply (VCC1)

4.1.1.2. The Reference Design of Regulator Outputs Power on PCBA is as Follows:

（1）The VDDD/VDDDIF/VCL voltages are provided by internal power（Figure 12）;

（2）The capacitors of VDDD/VDDDIF/VCL need to be as close to FPC as possible（Figure 12）;

（3）The VCL of FPC1 don't need to be short to the VCL of FPC2 and FPC3（Figure 12）;

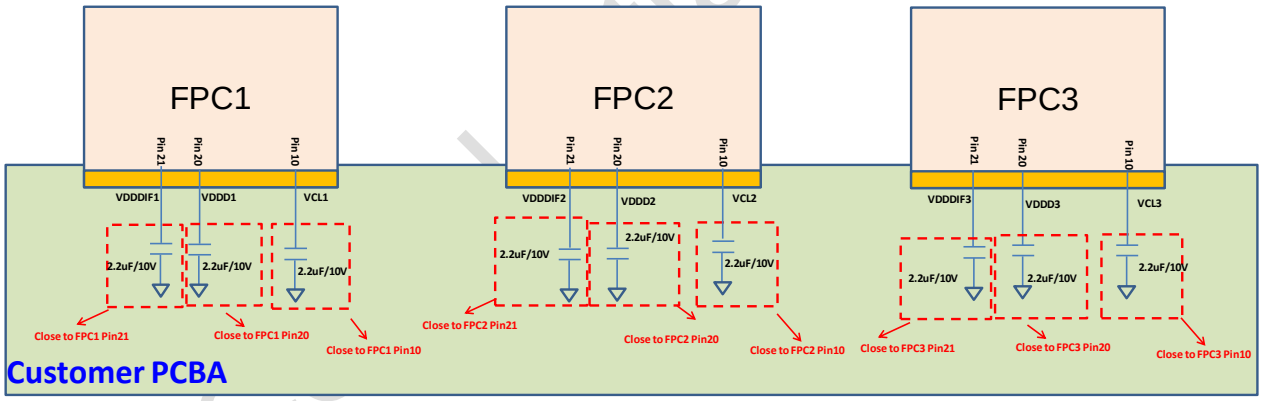


Figure 12: Cascade design for regulator outputs

（4）The VCOM voltages are provided by external power（Figure 13）;

（5）The capacitors of VCOM need to be as close to FPC as possible（Figure 13）;

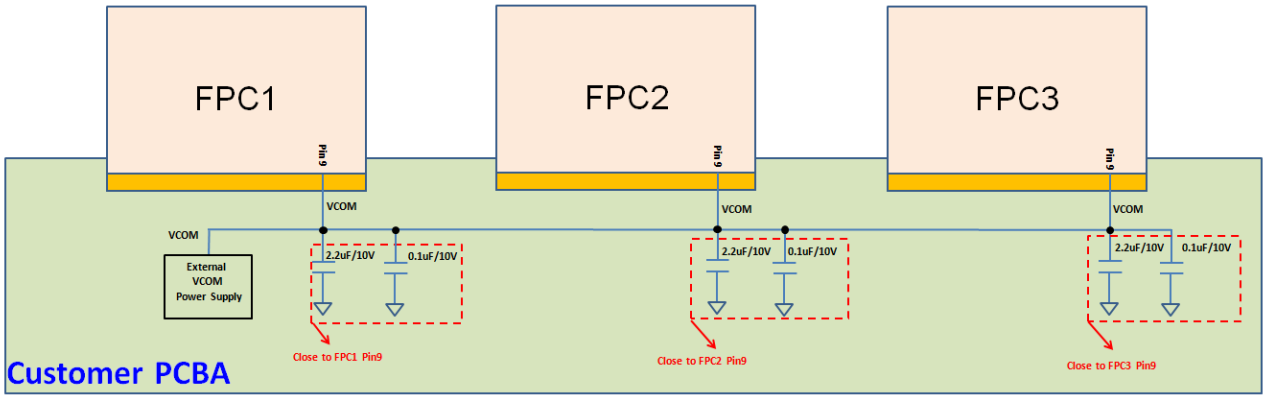


Figure 13: Cascade design with regulator outputs (VCOM)

4.1.1.3. The Reference Design of Gamma Reference Voltages on PCBA is as Follows:

（1）The gamma reference voltages are provided by internal power（Figure 14）;

（2）The capacitors of gamma reference voltages need to be as close to FPC1 as possible（Figure 14）;

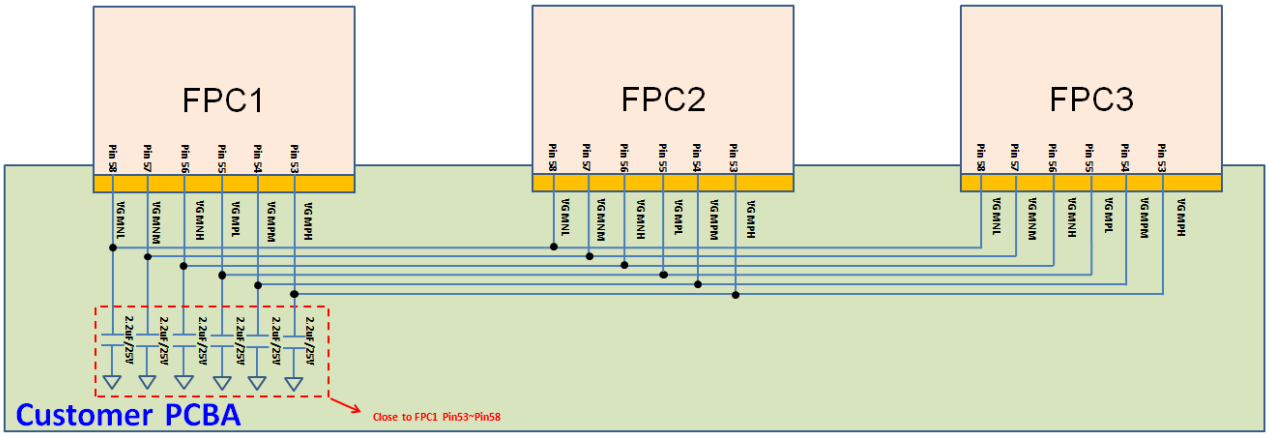


Figure 14: Cascade design for gamma reference voltages

4.1.1.4. The Reference Design of Signal on PCBA is as Follows:

（1）L type is recommended for LVDS trace（Figure 15）;

（2）The terminal resistors is placed to the LVDS trace terminal（Figure 15）;

（3）The resistance value of the terminal resistors is recommended as 100ohm （Figure 15）;

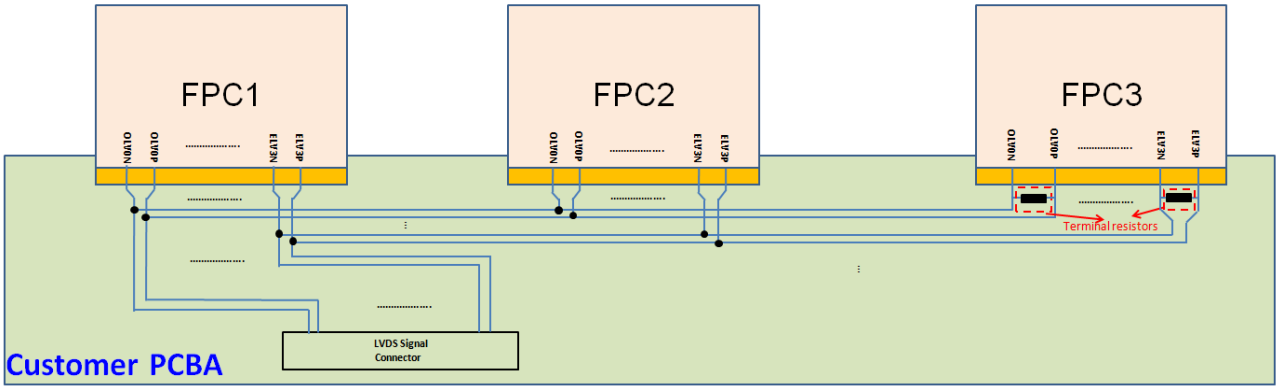


Figure 15: Cascade design with LVDS Signal

4.2 Signal Electrical Characteristics

4.2.1 Signal Electrical Characteristics For LVDS Receiver

The built-in LVDS receiver is compatible with (ANSI/TIA/TIA-644) standard.

Table 7 LVDS Receiver Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Differential Input High Threshold	Vth	-	-	(+0.2)	V	V_{CM}=1.2V
Differential Input Low Threshold	Vtl	(-0.2)	-	-	V	-
Magnitude Differential Input	$\|V_{ID}\|$	(0.2)	-	(0.6)	V	-
Common Mode Voltage	V_{CM}	(1)	(1.2)	(1.7-$\|V_{ID}\|$/2)	V	-
LVDS input voltage	VINLV	(0.7)	-	(1.7)	V	-
Differential input leakage	Ilvleak	(-10)	-	(+10)	uA	-

Note (1) Input signals shall be low or Hi- resistance state when VDD is off.

Note (2) All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD.

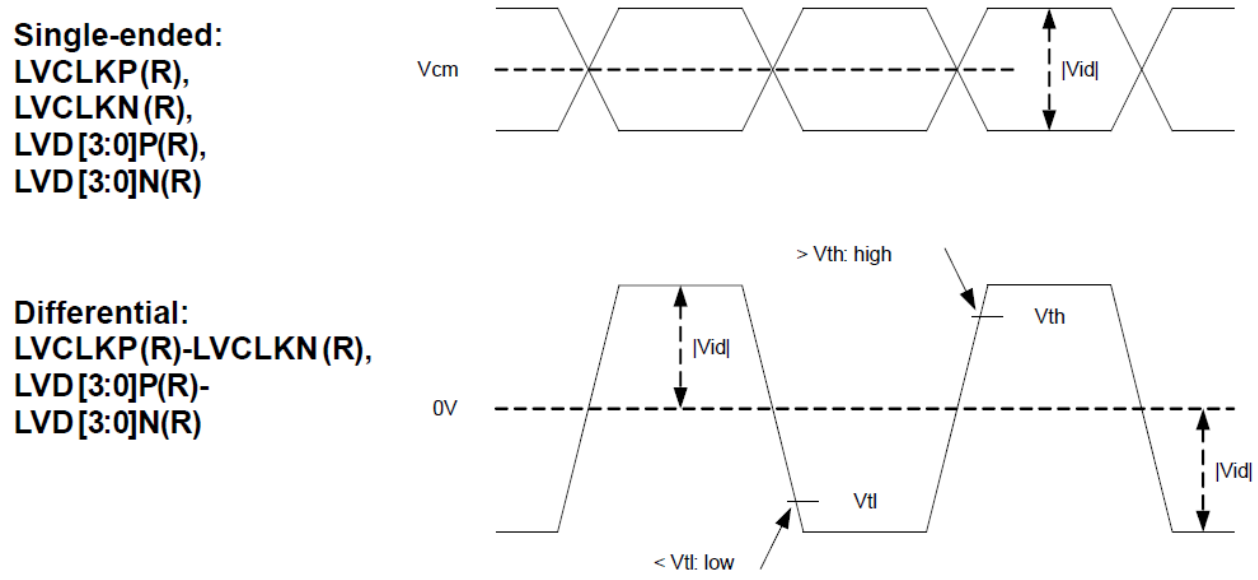


Figure 9 Voltage Definitions

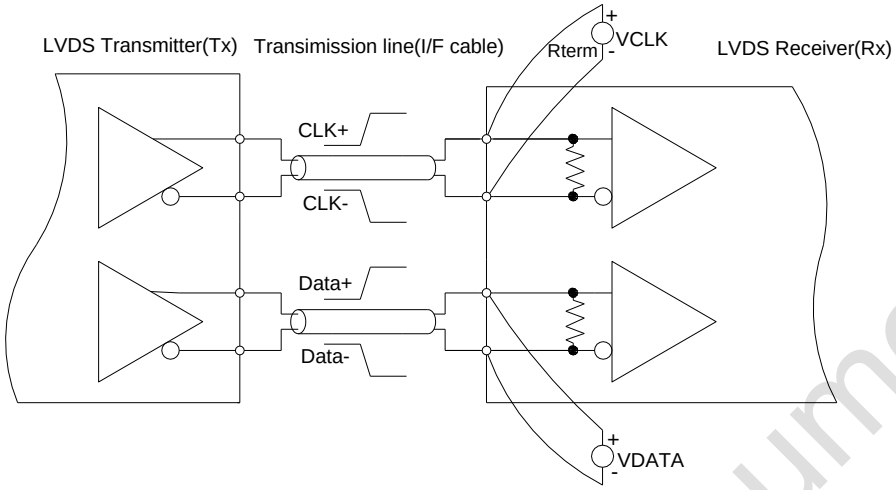


Figure 10 Measurement System

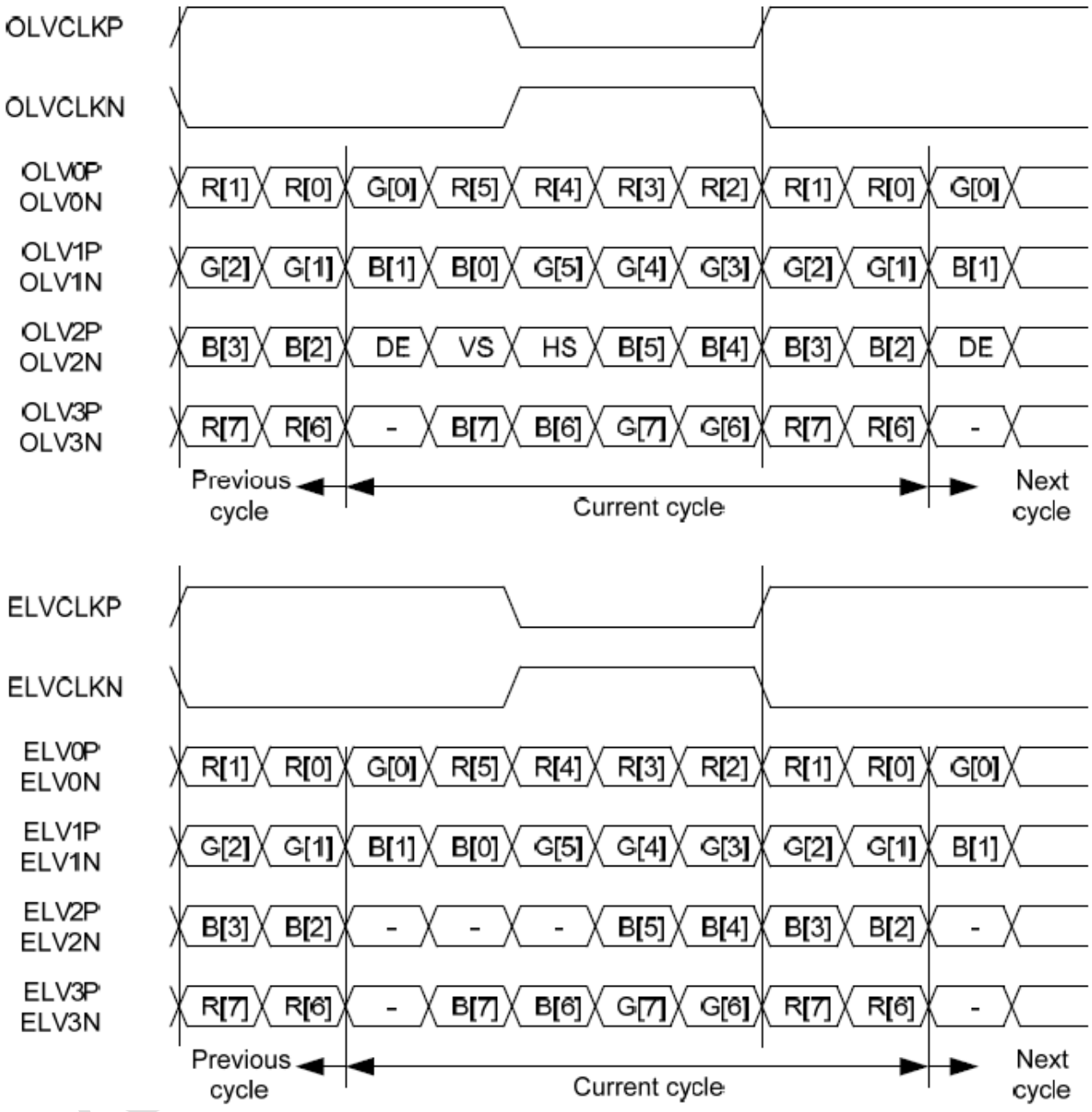
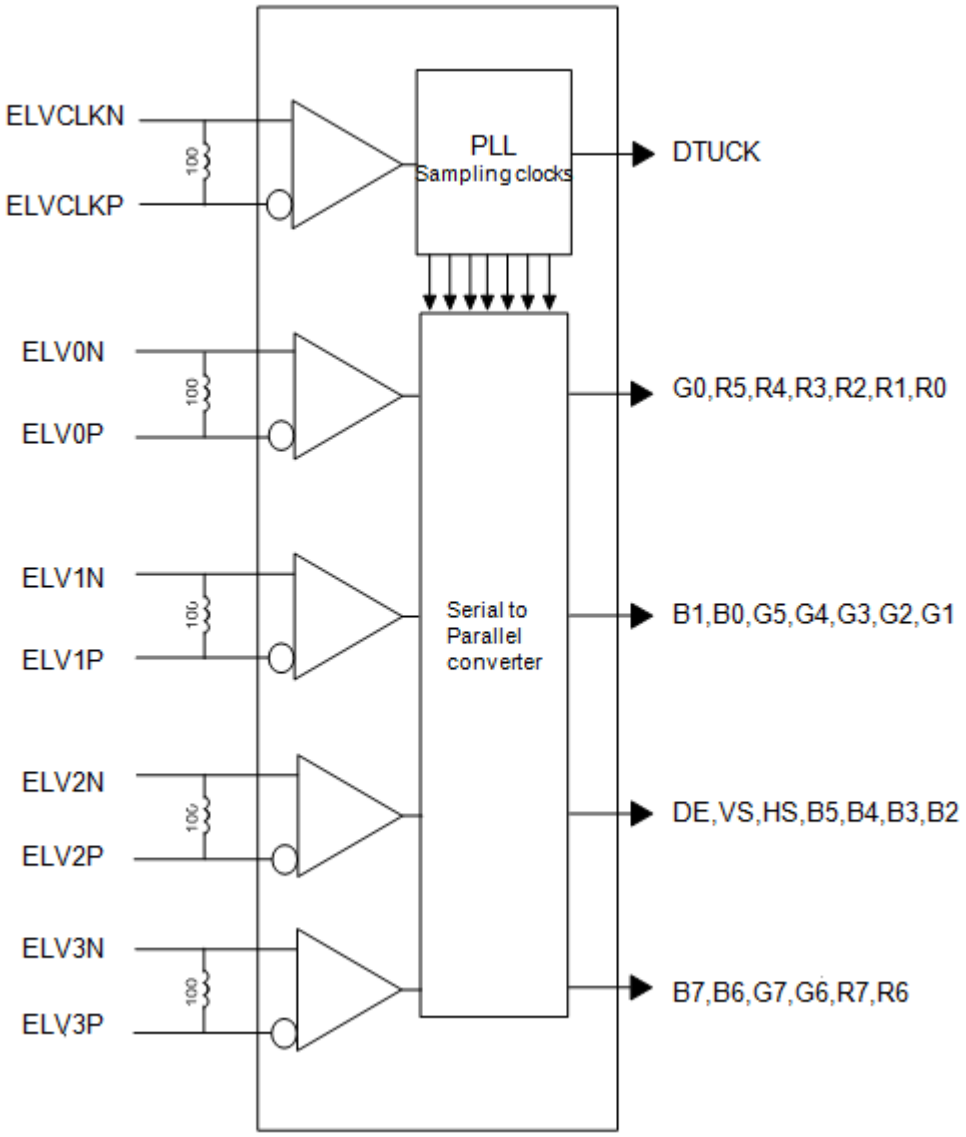


Figure 11 Data Mapping

4.2.2 LVDS Receiver Internal Circuit

Figure 12 shows the internal block diagram of the LVDS receiver. This LCD module equips termination resistors for LVDS link.



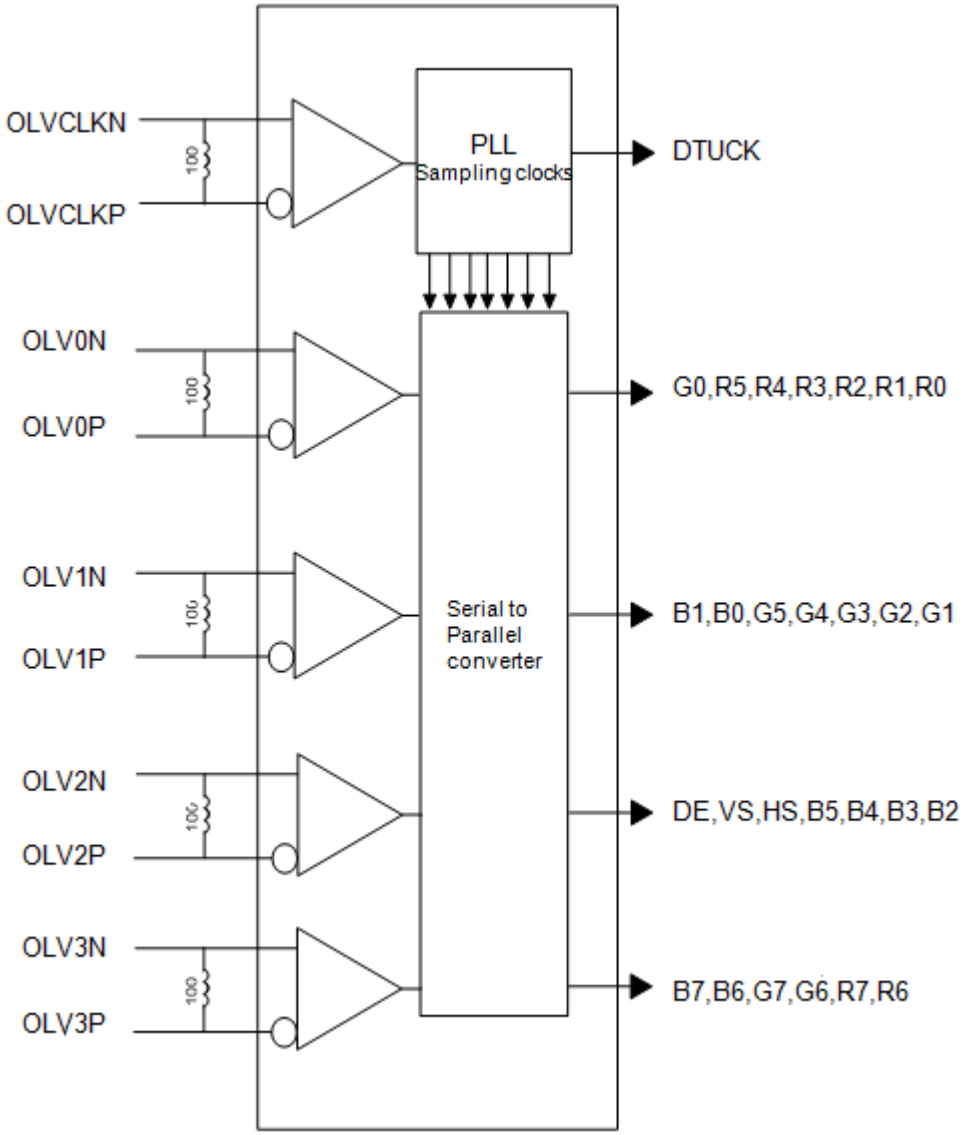


Figure 12 LVDS Receiver Internal Circuit

4.3 Interface Timings

Table 8 Interface Timings

Parameter	Symbol	Min.	Typ.	Max.	Unit
LVDS Clock Frequency	Fclk	(43.4)	(44.1)	(58.0)	MHz
H Total Time	HT	(990)	(1,002)	(1200)	Clocks
H Active Time	HA		(960)		Clocks
V Total Time	VT	(730)	(733)	(806)	Lines
V Active Time	VA		(720)		Lines
Frame Rate	FV	55	60	65	Hz

Note1：HT * VT *Frame Frequency≤58.0MHz

Note2：Dual link LVDS

Note3：All reliabilities are specified for timing specification based on refresh rate of 60Hz.

4.4 Input Power Specifications

Input power specifications are as follows.

Table 9 Input Power Specifications

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
System Power Supply							
LCD Drive Voltage (Logic)		VCC1	(3.0)	(3.3)	(3.6)	V	(1),(2)
VCC Current	White Pattern	I_{VCC1}	-	-	(70)	mA	(1),(4)
VCC Power Consumption	White Pattern	P_{VCC1}	-	-	(231)	mW	
Gate IC input High Voltage		VGH	(14)	(15)	(16)	V	(1)(2)
Gate IC Analog input current	White Pattern	I_{VGH}	-	-	(0.8)	mA	
Gate IC Analog Power Consumption		P_{VGH}	-	-	(12)	mW	
Gate IC input Low Voltage		VGL	(-12)	(-11)	(-10)	V	
Gate IC Analog input current	White Pattern	I_{VGL}	-	-	(0.8)	mA	(1)(2)
Gate IC Analog Power Consumption		P_{VGL}	-	-	(8.8)	mW	
Source IC Analog input voltage		VSP	(5.3)	(5.4)	(5.5)	V	(1)(3)
Source IC Analog input current	White	I_{VSP}	-	-	(40)	mA	
Source IC Analog Power Consumption		P_{VSP}	-	-	(216)	mW	(1)(3)
Source IC Analog input voltage		VSN	(-5.5)	(-5.4)	(-5.3)	V	(1)
Source IC Analog input current	White	I_{VSN}	-	-	(40)	mA	(1)
Source IC Analog Power Consumption		P_{VSN}	-	-	(216)	mW	(1)(3)
Panel Common Voltage		VCOM	(-1.75)	(-0.75)	(0.25)	V	(3)
Differential Impedance		Zm	(90)	(100)	(110)	Ω	(5)
Logic Input Signal High Level Voltage		VIH	(2.6)	-	(3.6)	V	(6)

Logic Input Signal Low Level Voltage	VIL	(0)	-	(0.5)	V	(6)

Note (1) All of the specifications are guaranteed under normal conditions. Normal conditions are defined as follow: Temperature: 25℃, Humidity: 55± 10%RH.

Note (2) All of the absolute maximum ratings specified in the table, if exceeded, may cause faulty operation or unrecoverable damage. It is recommended to follow the typical value.

Note (3) The specified V_{cc} current and power consumption are measured under the V_{cc1} = 3.3 V, FV= 60 Hz condition and White pattern.

Note (4) The figures below is the measuring condition of V_{cc1}. Rush current can be measured when T_{RUSH} is 0.5 ms.

Note (5)This impedance value is needed for proper display and measured from LVDS Tx to the mating connector.

Note (6)Logic input signal include BISTEN、TB、RL、RESETB、STBYB

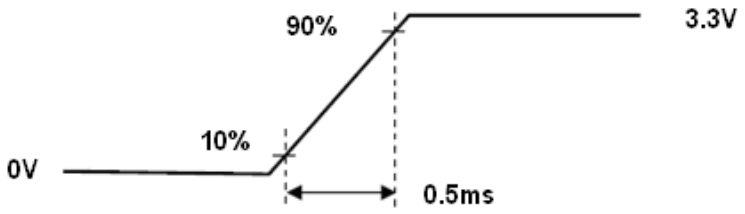


Figure 13 V_{cc1} Rising Time

4.5 Power ON/OFF Sequence

1.Interface signals are also shown in the chart. Signals from any system shall be Hi-resistance state or low level when VCC1 voltage is off.

2. When system first start up, should keep the VCC1 high time longer than 200ms, otherwise may cause image sticking when Vcc drop off.

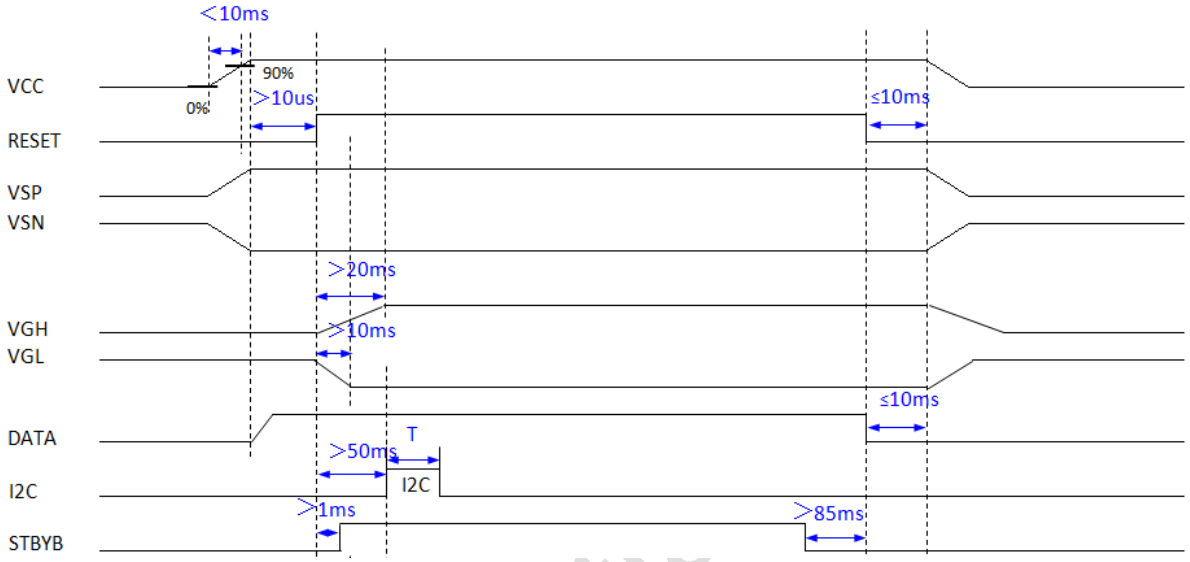
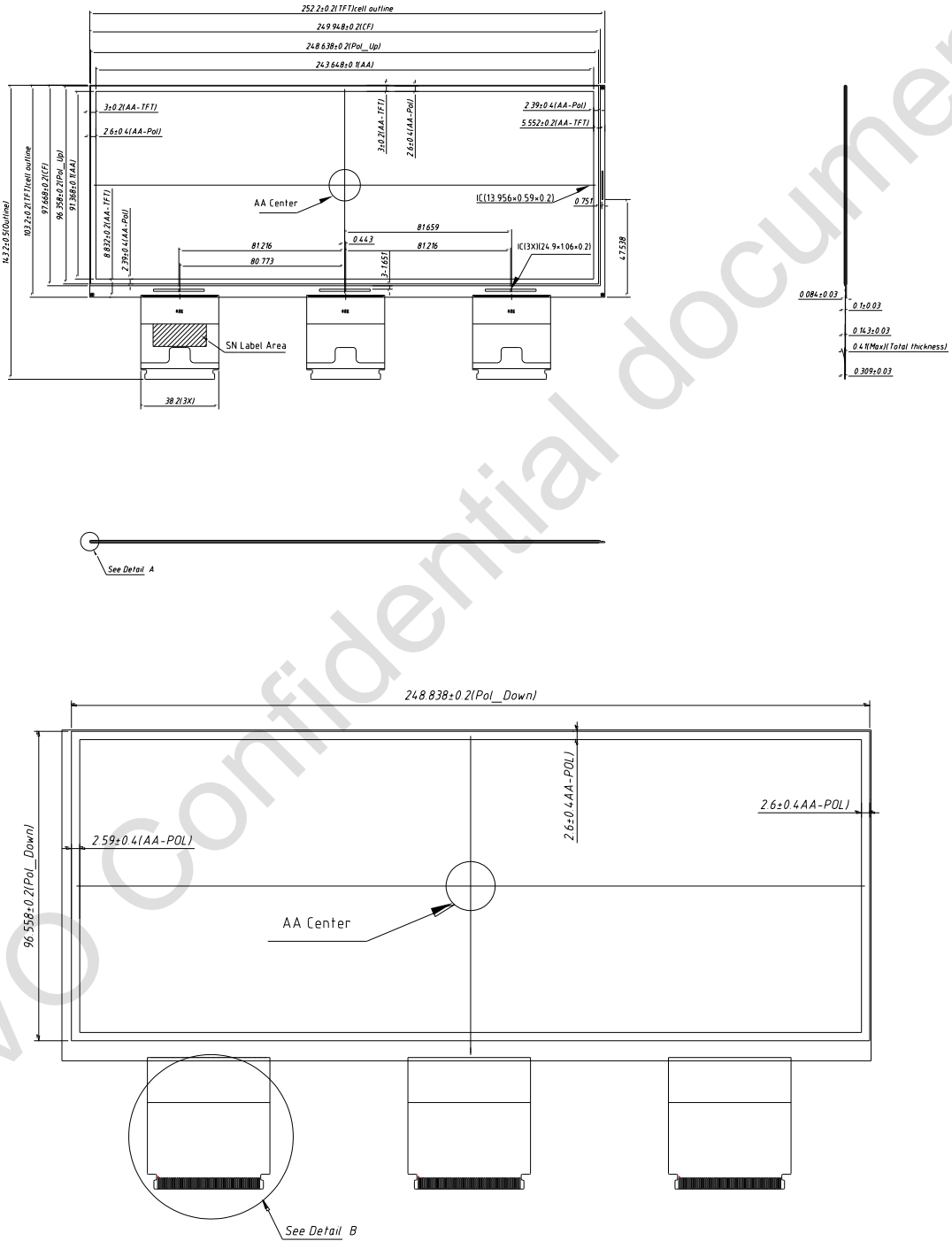


Figure 14 Power Sequence

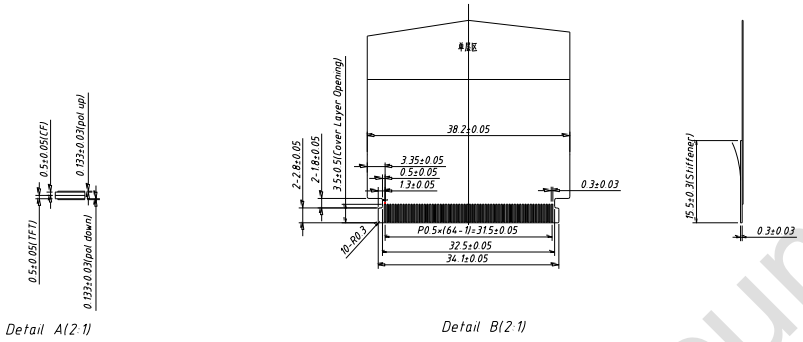
Note: T is On behalf of the time of code.

5.0 Mechanical Characteristics

5.1 Outline Drawing



FPC 3 **FPC 2** **FPC 1**



Unit: mm

Figure 15 Reference Outline Drawing

5.2 Dimension Specifications

Table 10 Module Dimension Specifications

Item	Min.	Typ.	Max.	Unit
Width	(252.00)	(252.20)	(252.40)	mm
Height	(103.00)	(103.20)	(103.40)	mm
Thickness	-	-	(1.426)	mm
Weight	-	-	(95)	g

Note：Outline dimension measure instrument: Vernier Caliper.

6.0 Reliability Conditions

Table 11 Reliability Condition

Item		Package	Test Conditions		Note
High Temperature/High Humidity Operating Test		FOG	T_{gs}=60℃, 90%RH, 240 hours		(1),(2),(3),(4)
High Temperature/High Humidity Storage Test		FOG	T_a=60℃, 90%RH, 240 hours		
High Temperature Operating Test		FOG	T_{gs}= 70℃, 240 hours		
Low Temperature Operating Test		FOG	T_a= -20℃, 240 hours		
High Temperature Storage Test		FOG	T_a= 85℃, 240 hours		(1),(3),(4)
Low Temperature Storage Test		FOG	T_a= -30℃, 240 hours		
Thermal Shock Non-operating Test		FOG	-20°(0.5hr)~70°(0.5hr)C/200cycles		
ESD Test	Operating	FOG	Contact	±4KV, 150pF(330Ohm)	(1),(2),(6)
			Air	±4KV, 150pF(330Ohm)	

Note (1) A sample can only have one test. Outward appearance, image quality and optical data can only be checked at normal conditions according to the IVO document before reliable test. Only check the function of the module after reliability test.

Note (2) The setting of electrical parameters should follow the typical value before reliability test.

Note (3) During the test, it is unaccepted to have condensate water remains. Besides, protect the module from static electricity.

Note (4) The sample must be released for 24 hours under normal conditions before judging. Furthermore, all the judgment must be made under normal conditions. Normal conditions are defined as follow: Temperature: 25℃, Humidity: 55± 10%RH. T_a= Ambient Temperature, T_{gs}= Glass Surface Temperature.

Note (5) The module should be fixed firmly in order to avoid twisting and bending.

Note (6) It could be regarded as pass, when the module recovers from function fault caused by ESD after resetting.

7.0 Package Specification

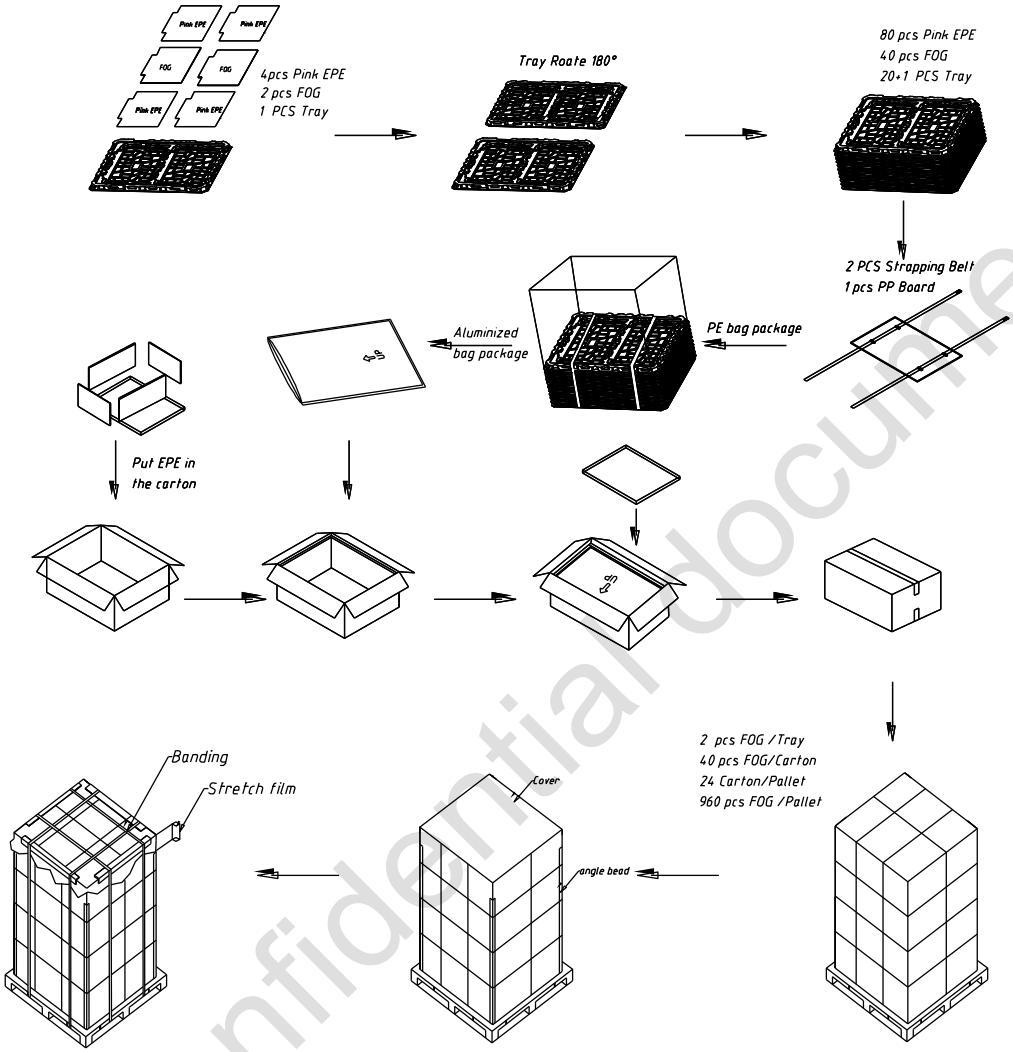
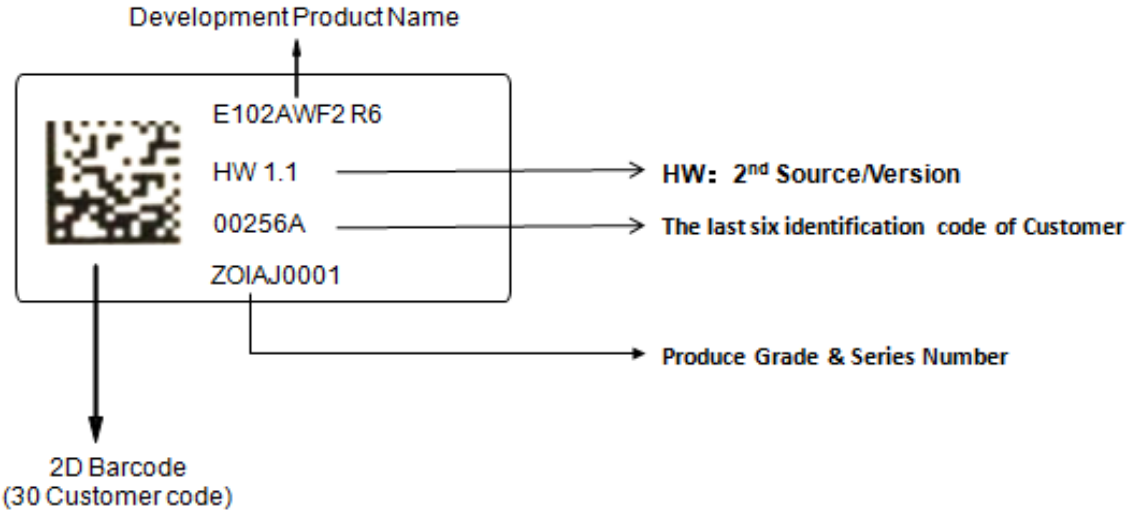


Figure 17 Packing Method

8.0 Lot Mark



Note: This picture is only an example.

8.1 30 Customer Code

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30

Code 1~6 : The last six identification code of Customer .

Code 7 : Space mark.

Code 8~22 : Module number、location information.

Code 23 :The Production Factory.

Code 24~26: Production Year ~ Month ~ Day.

Year	2006	2007	2008	2009	2010	2011	2012	2013	.....	2035
Mark	6	7	8	9	A	B	C	D	.....	Z

Month	Jan.	Feb.	Mar.	Apr.	May.	Jun.	Jul.	Aug.	Sep.	Oct	Nov.	Dec.
Mark	1	2	3	4	5	6	7	8	9	A	B	C

Day	1.	2.	3	4.	5	6	7	8	9	10	.....	31
Mark	1	2	3	4	5	6	7	8	9	A	.....	V

Coe 27~30: Series number.

9.0 General Precaution

9.1 Using Restriction

This product is not authorized for using in life supporting systems, aircraft navigation control systems, military systems and any other appliance where performance failure could be life-threatening or lead to be catastrophic.

9.2 Operation Precaution

(1)The LCD product should be operated under normal conditions.
Normal conditions are defined as below:

Temperature: 25℃

Humidity: 55±10%

Display pattern: continually changing pattern (Not stationary)

(2) Brightness and response time depend on the temperature. (It needs more time to reach normal brightness in low temperature.)

(3) It is necessary for you to pay attention to condensation when the ambient temperature drops suddenly. Condensate water would damage the polarizer and electrical contacted parts of the module. Besides, smear or spot will remain after condensate water evaporating.

(4) If the absolute maximum rating value was exceeded, it may damage the module.

(5) Do not adjust the variable resistor located on the module.

(6) Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding may be important to minimize the interference.

(7) Image sticking may occur when the module displayed the same pattern for long time.

(8) Do not connect or disconnect the module in the “power on” condition. Power supply should always be turned on/off by the “power on/off sequence”

(9) Ultra-violet ray filter is necessary for outdoor operation.

9.3 Mounting Precaution

(1) All the operators should be electrically grounded and with Ion-blown equipment turning on when mounting or handling. Dressing finger-stalls out of the gloves is important for keeping the panel clean during the incoming inspection and the process of assembly.

(2) It is unacceptable that the material of cover case contains acetic or chloric. Besides, any other material that could generate corrosive gas or cause circuit break by electro-chemical reaction is not desirable.

(3) The case on which a module is mounted should have sufficient strength so that external force is not transmitted to the module directly.

(4) It is obvious that you should adopt radiation structure to satisfy the temperature specification.

(5) It should be attached to the system tightly by using all holes for mounting, when the module is assembled. Be careful not to apply uneven force to the module，especially to the PCB on the back.

(6) A transparent protective film needs to be attached to the surface of the module.

(7) Do not press or scratch the polarizer exposed with anything harder than HB pencil lead. In addition, don't touch the pin exposed with bare hands directly.
(8) Clean the polarizer gently with absorbent cotton or soft cloth when it is dirty.
(9) Wipe off saliva or water droplet as soon as possible. Otherwise, it may cause deformation and fading of color.
(10) Desirable cleaners are IPA (Isopropyl Alcohol) or hexane. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(11) Do not disassemble or modify the module. It may damage sensitive parts in the LCD module, and cause scratches or dust remains. IVO does not warrant the module, if you disassemble or modify the module.

9.4 Handling Precaution

(1) Static electricity will generate between the film and polarizer, when the protection film is peeled off. It should be peeled off slowly and carefully by operators who are electrically grounded and with Ion-blown equipment turning on. Besides, it is recommended to peel off the film from the bonding area.
(2) The protection film is attached to the polarizer with a small amount of glue. When the module with protection film attached is stored for a long time, a little glue may remain after peeling.
(3) If the liquid crystal material leaks from the panel, keep it away from the eyes and mouth. In case of contact with hands, legs or clothes, it must be clean with soap thoroughly.

9.5 Storage Precaution

When storing modules as spares for long time, the following precautions must be executed.
(1) Store them in a dark place. Do not expose to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.
(2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.
(3) It is recommended to use it in a short-time period, after it's unpacked. Otherwise, we would not guarantee the quality.

9.6 Others

When disposing LCD module, obey the local environmental regulations.