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Ver.	Date	Revised Content/Summary	Page	Revised By
00	2022/3/25	Tentative	All	朱婷婷

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1.0 General Descriptions

1.1 Introduction

The T146AW41 R0 is a Color Active Matrix Liquid Crystal Display with In Cell and a back light and Cover glass system. The matrix uses a-Si Thin Film Transistor as a switching device. This TFT LCD has a 14.6 inch diagonally measured active display area with FHD resolution (1920 horizontal by 1440 vertical pixels array).

1.2 Features

- ■ Supported FHD Resolution
- ■ LVDS Interface
- ■ Wide View Angle
- ■ Compatible with RoHS Standard

1.3 Product Summary

Items	Specifications	Unit
Screen Diagonal	14.6	inch
Active Area (H x V)	297.60 x 223.20	mm
Number of Pixels (H x V)	1,920 x 1,440	-
Pixel Pitch (H x V)	0.1550 x 0.1550	mm
Pixel Arrangement	R.G.B. Vertical Stripe	-
Display Mode	Normally Black	-
White Luminance	(650) (Typ.)	cd /m^2
Contrast Ratio	(1,500) (Typ.)	-
Response Time	(25) (Max.) @25℃	ms
Input Voltage	3.3 (Typ.)	V
Power Consumption	TBD	W
Weight	(1,042) (Max.)	g
Outline Dimension(H x V x D)	(314.6) (Typ.) x (244.4) (Typ.) x (10.14) (Max.)	mm
Electrical Interface (Logic)	LVDS	-
Support Color	16.7 M	-
NTSC	85 (Typ.)	%
TP Mode	In Cell	-
Sensor Interface	I^2C	-
Report Rate	60	Hz
CG type	244.4 x 314.6	mm
CG Surface Hardness	3H(min)	-
CG Surface treatment:	AG/AR/AF	-
反射率	≤1.5	%

色差(黑框/显示区)	≤1.5	Δ E

1.4 Functional Block Diagram

Figure 1 shows the functional block diagram of the LCD module.

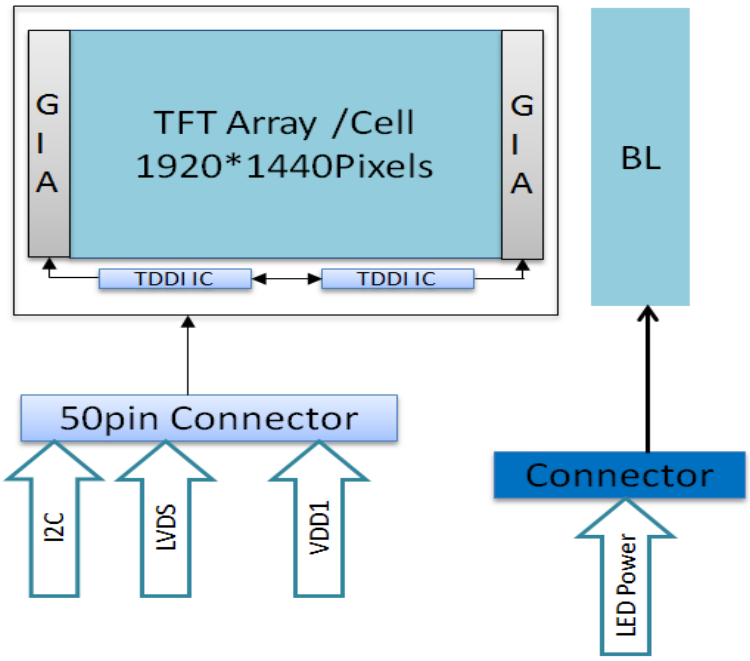


Figure 1 Block Diagram

1.5 Pixel Mapping

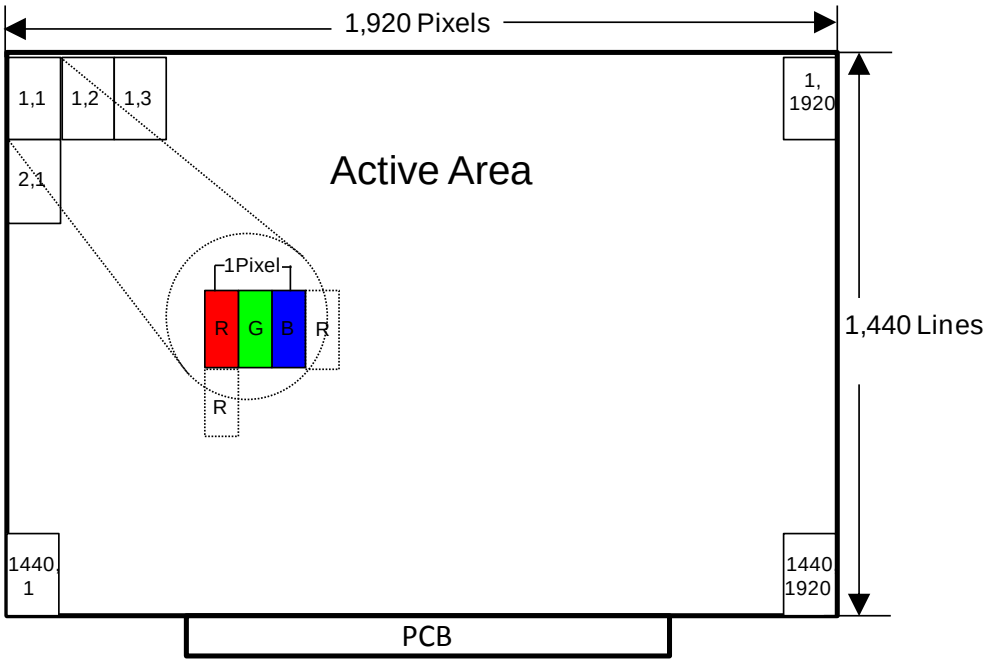


Figure2 Pixel Mapping

2.0 Absolute Maximum Ratings

Table 1 Electrical & Environment Absolute Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage (System power supply)	VDD1	(-0.3)	(3.9)	V	(1),(2), (3),(4)
Logic Input Signal Voltage	V_{Signal}	(-0.3)	(3.9)	V	
Operating Temperature	T_{gs}	(-30)	(85)	℃	
Storage Temperature	T_a	(-40)	(95)	℃	

Note (1) All the parameters specified in the table are absolute maximum rating values that may cause faulty operation or unrecoverable damage, if exceeded. It is recommended to follow the typical value.

Note (2) All the contents of electro-optical specifications and display fineness are guaranteed under Normal Conditions. All the display fineness should be inspected under normal conditions. Normal conditions are defined as follow: Temperature: 25℃, Humidity: 55± 10%RH.

Note (3) Unpredictable results may occur when it was used in extreme conditions. T_a= Ambient Temperature, T_{gs}= Glass Surface Temperature. All the display fineness should be inspected under normal conditions.

Note (4) Temperature and relative humidity range are shown in the figure below. Wet bulb temperature should be lower than 57.8℃, and no condensation of water. Besides, protect the module from static electricity.

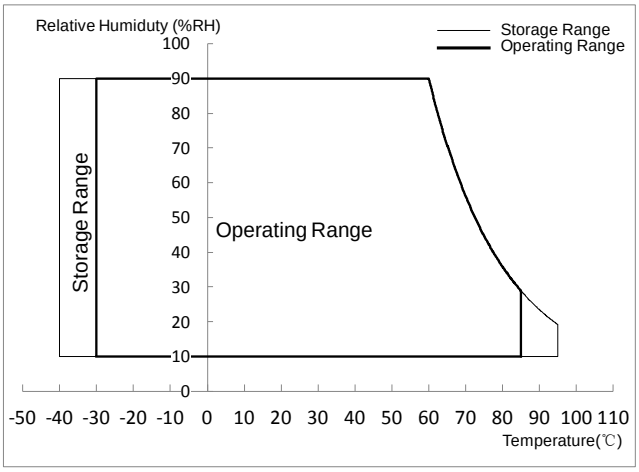


Figure 3 Absolute Ratings of Environment of the LCD Module

3.0 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes.

Table 2 Optical Characteristics

Item	Conditions		Min.	Typ.	Max.	Unit	Note
Viewing Angle （CR≥10）	Horizontal	θ_{x+}	(85)	TBD	-	degree	(1),(2),(3),(4)(8)
		θ_{x-}	(85)	TBD	-		
	Vertical	θ_{y+}	(85)	TBD	-		
		θ_{y-}	(85)	TBD	-		
Contrast Ratio	Center		TBD	(1,500)	-	-	(1),(2),(4),(8) θx=θy=0°
Response Time	Rising + Falling		-	TBD	(25)	ms	(1),(2),(5),(8) θx=θy=0°
Color Chromaticity (CIE1931)	Red x		Typ. -0.03	(0.665)	Typ. +0.03	-	(1),(2),(3),(8) θx=θy=0°
	Red y			(0.307)		-	
	Green x			(0. 303)		-	
	Green y			(0.654)		-	
	Blue x			(0.149)		-	
	Blue y			(0. 057)		-	
	White x			(0.307)		-	
	White y			(0.315)		-	
NTSC	-		(80)	(85)	-	%	(1),(2),(3),(8) θx=θy=0°
White Luminance	Center Point		TBD	(650)	-	cd/m^2	(1),(2),(6),(8) θx=θy=0°
Luminance Uniformity	9 Points		(75)	(80)	-	%	(1),(2),(7),(8) θx=θy=0°

Note (1) Measurement Setup:

The LCD module should be stabilized at given ambient temperature (25℃) for 30 minutes to avoid abrupt temperature changing during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 30 minutes in the windless room.

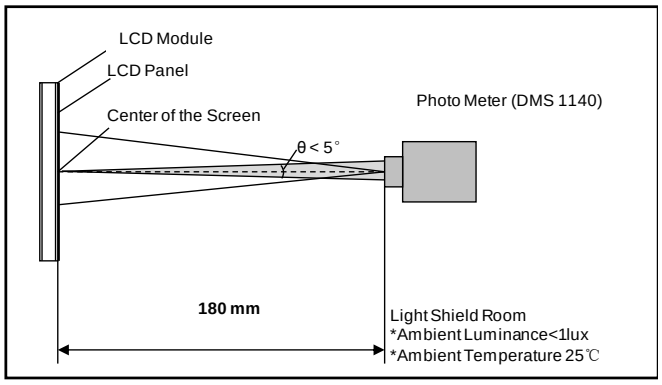


Figure 4 Measurement Setup

Note (2) The LED input parameter setting as:

I_{LED}: 195mA

Note (3) Definition of Viewing Angle

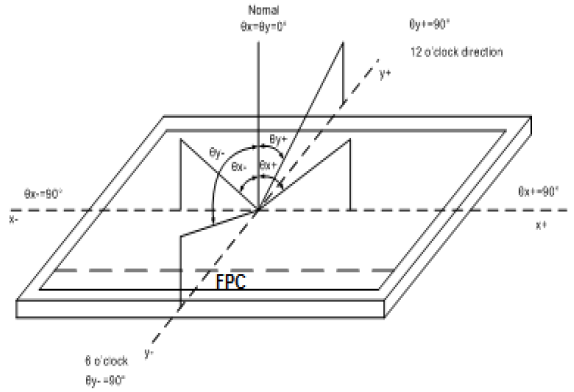


Figure 5 Definition of Viewing Angle

Note (4) Definition of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression:

Contrast Ratio (CR) = The luminance of White pattern/ The luminance of Black pattern

Note (5) Definition of Response Time (T_R, T_F)

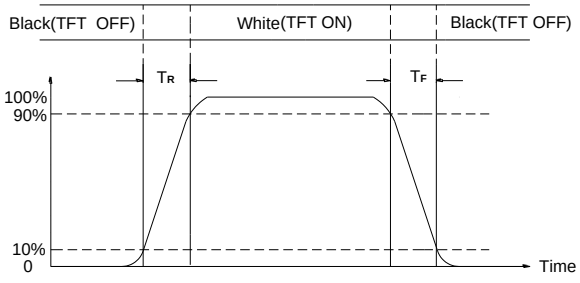


Figure 6 Definition of Response Time

Note (6) Definition of Luminance of White

Measure the luminance of White pattern (Ref.: Active Area)

Display Luminance=L1（center point）

H—Active Area Width, V—Active Area Height, L—Luminance

Note (7) Definition of Luminance Uniformity (Ref.: Active Area)

Measure the luminance of White pattern at 9 points.

Luminance Uniformity= Min.(L1, L2, ... LX) / Max.(L1, L2, ... LX)

H—Active Area Width, V—Active Area Height, L—Luminance

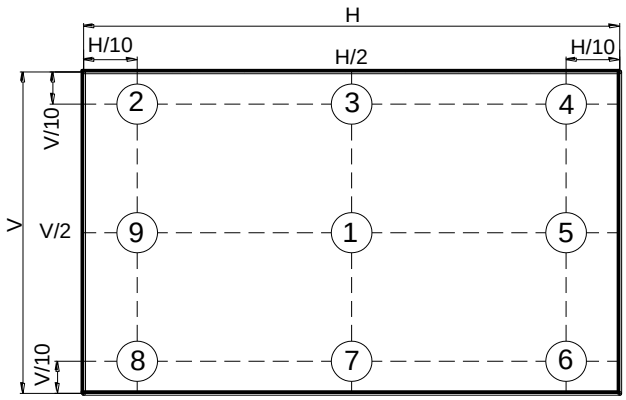


Figure 7 Measurement Locations of 9 Points

Note (8) All optical data are based on IVO given system & nominal parameter & testing machine in this document.

4.0 Electrical Characteristics

4.1 Interface Connector

Table 3 Signal Connector Type

Item	Description
Mating Receptacle / Type (Reference)	STM/FFSKL05007G50G

Table 4 Signal Connector Pin Assignment

Pin No.	Symbol	Description	Remarks
1	OTP_PVPP	EXT Power supply for OTP circuit (Normal 0V, OTP 7.25V±0.25V)	-
2	GND	Ground	-
3	DA_P_O_S	LVDS input For Slave1 IC	-
4	DA_N_O_S	LVDS input For Slave1 IC	-
5	GND	Ground	-
6	DB_P_O_S	LVDS input For Slave1 IC	-
7	DB_N_O_S	LVDS input For Slave1 IC	-
8	GND	Ground	-
9	DC_P_O_S	LVDS input For Slave1 IC	-
10	DC_N_O_S	LVDS input For Slave1 IC	-
11	GND	Ground	-
12	CLK_P_O_S	LVDS input For Slave1 IC	-
13	CLK_N_O_S	LVDS input For Slave1 IC	-
14	GND	Ground	-
15	DD_P_O_S	LVDS input For Slave1 IC	-
16	DD_N_O_S	LVDS input For Slave1 IC	-
17	GND	Ground	-
18	DA_P_O_M	LVDS input For Master IC	-
19	DA_N_O_M	LVDS input For Master IC	-
20	GND	Ground	-
21	DB_P_O_M	LVDS input For Master IC	-
22	DB_N_O_M	LVDS input For Master IC	-
23	GND	Ground	-
24	DC_P_O_M	LVDS input For Master IC	-
25	DC_N_O_M	LVDS input For Master IC	-

26	GND	Ground	-
27	CLK_P_O_M	LVDS input For Master IC	-
28	CLK_N_O_M	LVDS input For Master IC	-
29	GND	Ground	-
30	DD_P_O_M	LVDS input For Master IC	-
31	DD_N_O_M	LVDS input For Master IC	-
32	GND	Ground	-
33	VDD1	EXT power,3.3V (+/-0.3V)	-
34	NC	NC	-
35	NC	NC	-
36	GND	Ground	-
37	TP_I2C_SDA	I2C interface data signal for touch	-
38	TP_I2C_SCL	I2C interface data signal for touch	-
39	TP_I2C_INT	Touch screen interrupt line	-
40	TP_EXT_RSTN	Touch external reset signal	-
41	BIST_EN	Enable BIST Function(Normal 0V,BIST 3.3V)	-
42	TP_GPIO[0]	Used for low power wake up gesture function	-
43	PON	SLPIN/SLPOUT hardware control signal	-
44	TP_GPIO[1]	Inform LCD error information to SoC	-
45	RESX	DI-C is initialized when this pin is low	-
46	Fail_DET	Fail detection signal output	-
47	GND	Ground	-
48	DD_SDI_SDA	I2C interface Data signal use for OTP/Inform LCD error information to SoC	-
49	DD_SCL	I2C interface Data signal use for OTP/Inform LCD error information to SoC	-
50	GND	Ground	-

Table 5 LED Connector Name / Designation

Item	Description
Mating Receptacle / Type (Reference)	STM/FFSKL05007N12D

Table 6 LED Connector Pin Assignment

Pin No.	Symbol	Description	Remarks
1	LED-Pin1	LED_A	-
2	LED-Pin2	LED_A	-
3	LED-Pin3	LED_A	-
4	LED-Pin4	NC	-
5	LED-Pin5	NC	-
6	LED-Pin6	LED_K1	-
7	LED-Pin7	LED_K2	-
8	LED-Pin8	LED_K3	-
9	LED-Pin9	LED_K4	-
10	LED-Pin10	LED_K5	-
11	LED-Pin11	NTC+	
12	LED-Pin12	NTC-	

4.2 Signal Electrical Characteristics

4.2.1 Signal Electrical Characteristics For LVDS Receiver

Table 7 LVDS Receiver Input DC Specifications

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Positive-going input threshold voltage	V_{TH}	-	-	(90)	mV
Negative-going input threshold voltage	V_{TL}	(-90)	-	-	mV
LVDS differential voltage	$\|V_{ID}\|$	(90)	(350)	(800)	mV
LVDS input common mode voltage	V_{CMLY}	0.3+$\|V_{ID}\|$/ 2	-	2.3-$\|V_{ID}\|$/ 2	V

Note:(1)Requirement of termination resistance(Ω)：80(Min.)/100(Typ.)/120(Max).

(2)Test conditions: VCMLV=1.2V, VDD1=2.7V~3.6V

(3)Test condition: Test point is IC pad.

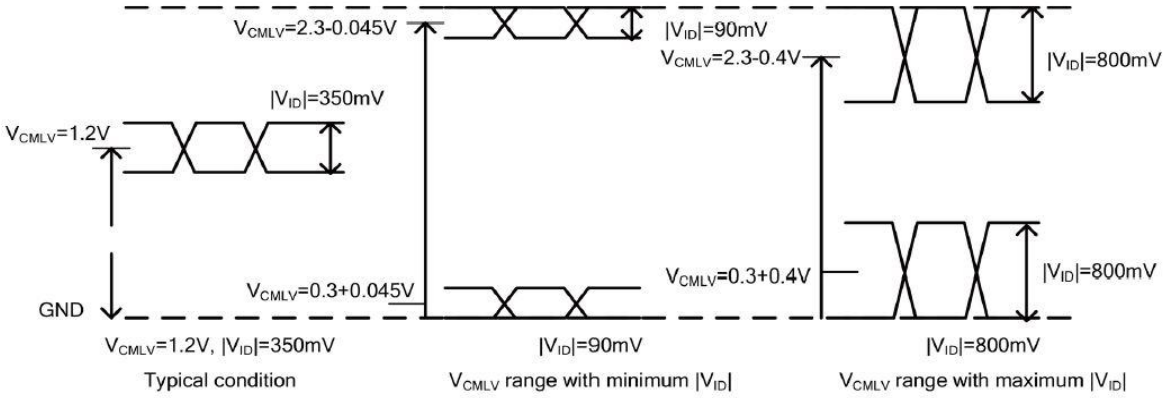


Figure 8 LVDS Receiver Input Signal levels

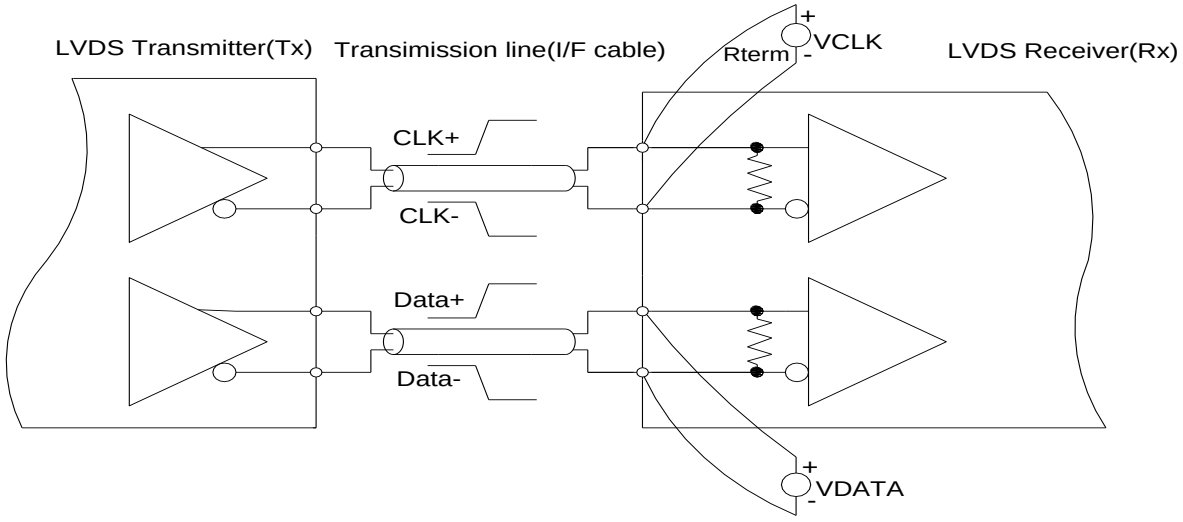


Figure 9 Measurement System

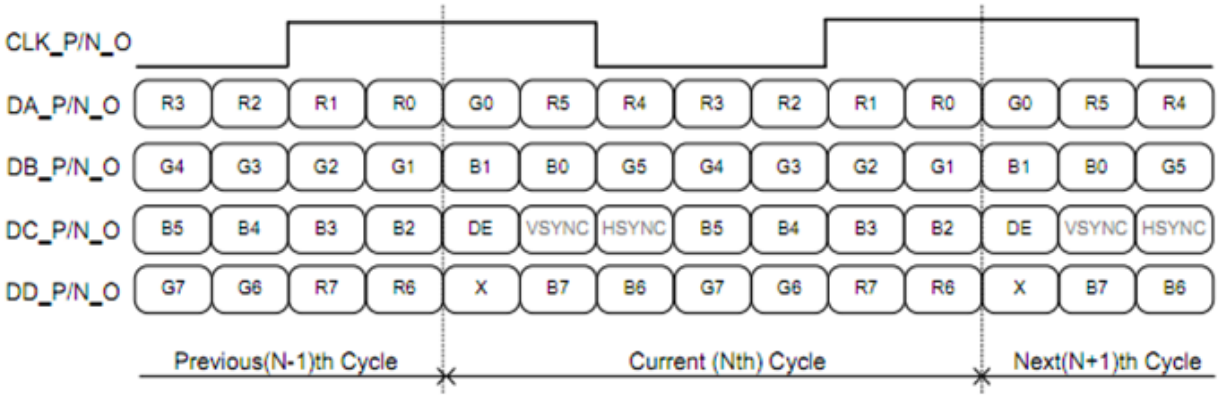


Figure 10 Data Mapping

4.2.2 AC Characteristics-1

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock frequency	F_{LVCYC}	-	-	140	MHZ
Clock period	T_{LVCYC}	7.14	-	-	ns
1 data bit time	UI	-	1/7	-	T_{LVCYC}
Input data position for bit0	T_{RIP0}	$-T_{EB}$	0	$+T_{EB}$	UI
Input data position for bit1	T_{RIP1}	$1-T_{EB}$	1	$1+T_{EB}$	UI
Input data position for bit2	T_{RIP2}	$2-T_{EB}$	2	$2+T_{EB}$	UI
Input data position for bit3	T_{RIP3}	$3-T_{EB}$	3	$3+T_{EB}$	UI
Input data position for bit4	T_{RIP4}	$4-T_{EB}$	4	$4+T_{EB}$	UI
Input data position for bit5	T_{RIP5}	$5-T_{EB}$	5	$5+T_{EB}$	UI
Input data position for bit6	T_{RIP6}	$6-T_{EB}$	6	$6+T_{EB}$	UI

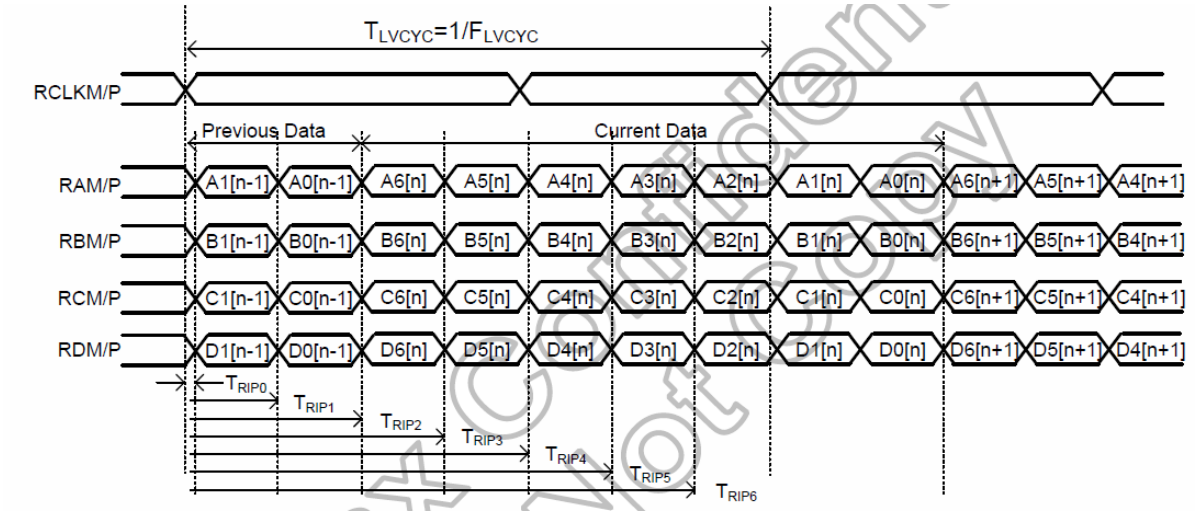


Figure 11 LVDS interface transmission flow

4.2.3 AC Characteristics-2

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Input eye border(LVDS＜100MHZ)	T_{EB}	-	-	0.25	UI
Input eye border(LVDS≥100MHZ)	T_{EB}	-	-	0.2	UI
Input eye width(LVDS＜100MHZ)	T_{EW}	0.5	-	-	UI
Input eye width(LVDS≥100MHZ)	T_{EW}	0.6	-	-	UI
Maximum deviation of input clock frequency during SSC	FDEW	-	-	±3(1)	%
Max./Min. modulation frequency of input clock during SSC	FMOD	15	-	200	KHZ

Note: (1) Test system with long cable may affect the SSC performance.

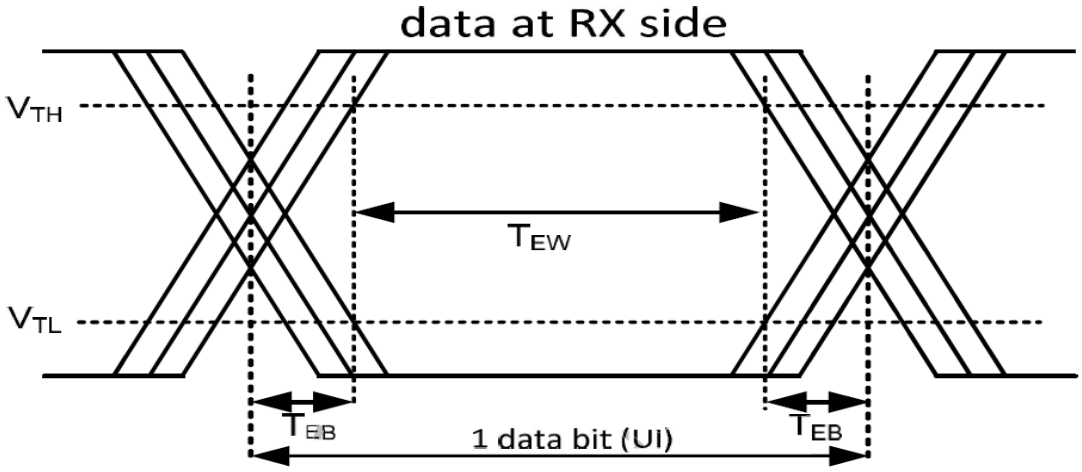


Figure 12 LVDS Input eye diagram

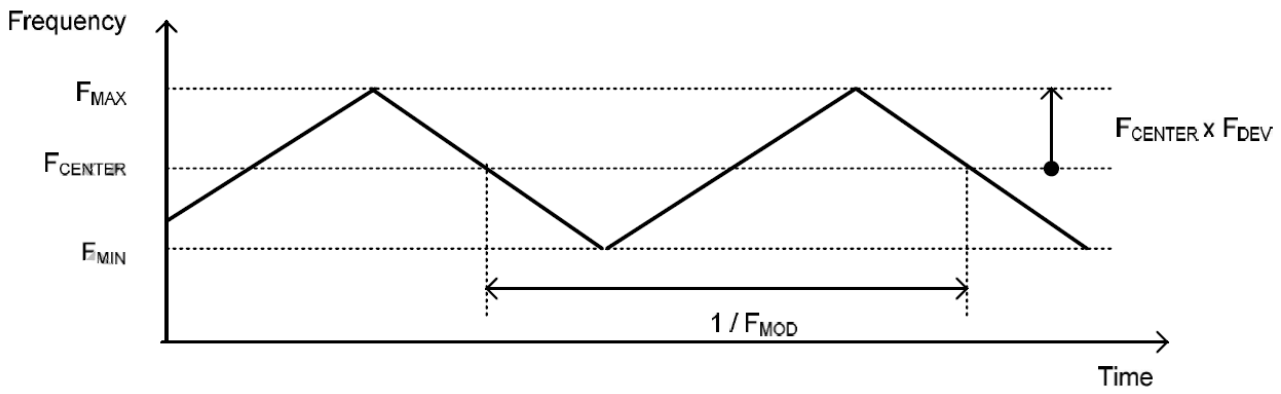


Figure 13 Spread spectrum

4.2.4 LVDS Receiver Internal Circuit

Figure 14 shows the internal block diagram of the LVDS receiver. This LCD module equips termination resistors for LVDS link.

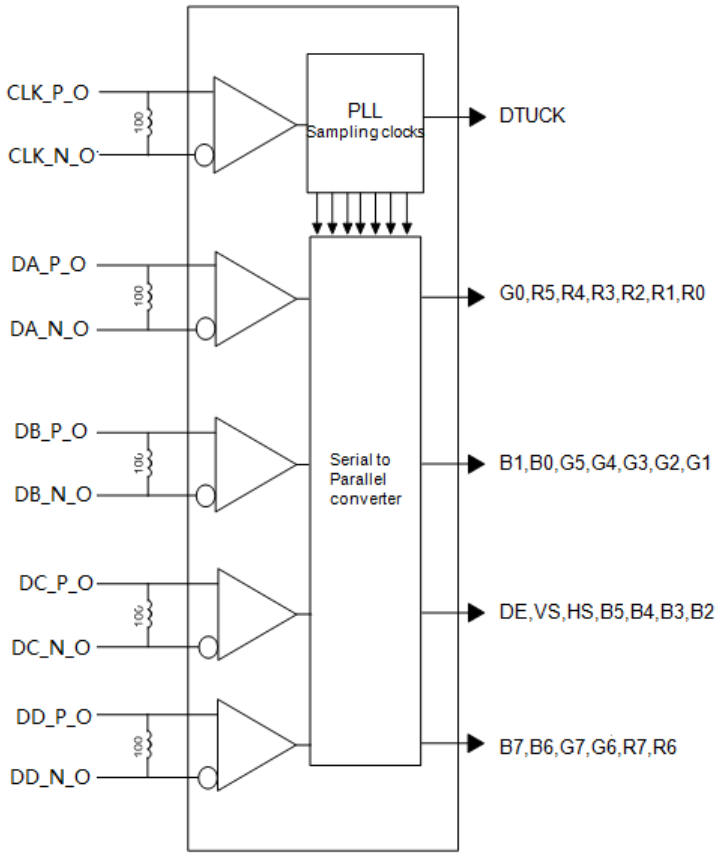


Figure 14 LVDS Receiver Internal Circuit

4.3 Interface Timings

Table 8 Interface Timings

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	Fdclk	(107.9)	(108.32)	(108.75)	MHz
Horizontal valid data	Thd		960		DCLK
Hsync pulse width	Thpw	(20)	(20)	(20)	DCLK
Hsync back porch	Thbp	(18)	(20)	(22)	DCLK
Hsync front porch	Thfp	(18)	(20)	(22)	DCLK
1 horizontal line	Th	(1,016)	(1,020)	(1,024)	DCLK
Vertical valid data	Tvd		1,440		H
Vsync pulse width	Tvpw	(2)	(2)	(2)	H
Vsync back porch	Tvbp	(8)	(8)	(8)	H
Vsync front porch	Tvfp	(320)	(320)	(320)	H
1 vertical field	Tv	(1,770)	(1,770)	(1,770)	H
Frame rate	FR	-	(60)	-	Hz

Note1：HT * VT *Frame Frequency≤108.75MHz

Note2: All reliabilities are specified for timing specification based on refresh rate of 60Hz.

T146AW41 R0 is secured only for function under lower refresh rate;

4.4 Input Power Specifications

Input power specifications are as follows.

Table 9 Input Power Specifications

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
System Power Supply							
LCD Drive Voltage (Logic)		VDD1	(3.0)	(3.3)	(3.6)	V	(1),(2)
VDD1 Current(White Pattern)		I_{VDD1}	-	-	(500.0)	mA	(1),(3)
VDD Power Consumption (White Pattern)		P_{VDD1}	-	-	(1.65)	W	
LCD Self Test (BIST)	High level voltage	V_{BIST}	(3.0)	-	(3.6)	V	(1)
	Low level voltage		(0)	-	(1.0)	V	
Rush Current		I_{Rush}	-	-	(1.0)	A	(1),(4)
Allowable Logic/LCD Drive Ripple Voltage		V_{VDD-RP}	-	-	TBD	mV	(1)

Input high-level voltage Applied Pins (All Input Pad with VDD1)	V_{IH}	0.7*VDD1	-	VDD1	V	
Input low-level voltage Applied Pins (All Input Pad with VDD1)	V_{IL}	0	-	0.3*VDD1	V	
Output high voltage VDD1=2.7~3.6 I_{OH}=1mA	V_{OH}	0.8*VDD1	-	-	V	
Output Low voltage VDD1=2.7~3.6 I_{OL}=1mA	V_{OL}	-	-	0.2*VDD1	V	
LED Power Supply						
LED Input Voltage	V_{LED}	(19.385)	-	(38.77)	V	(1),(2)
LED Power Consumption	P_{LED}	-	-	(20.46)	W	(1)
LED Forward Voltage	V_F	(2.7)	-	(3.1)	V	(1),(2)
LED Forward Current	I_F	-	(110)	-	mA	
LED Life Time	LT	(30,000)	-	-	Hours	(1)

Note (1) All of the specifications are guaranteed under normal conditions. Normal conditions are defined as follow: Temperature: 25℃, Humidity: 55± 10%RH.

Note (2) All of the absolute maximum ratings specified in the table, if exceeded, may cause faulty operation or unrecoverable damage.It is recommended to follow the typical value.

Note (3) The specified VDD1 current and power consumption are measured under the VDD1 = 3.3 V, FV= 60 Hz condition and White pattern.

Note (4) The figures below is the measuring condition of VDD1. Rush current can be measured when TRUSH is 0.5 ms.

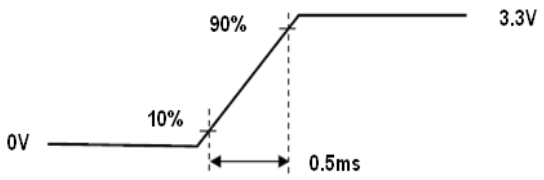


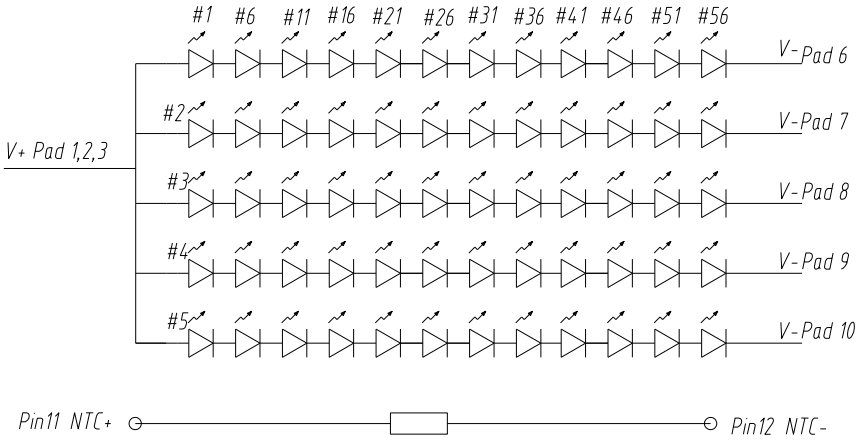
Figure 15 V_{DD} Rising Time

Note (5) The life time is determined as the sum of the lighting time till the luminance of LCD at the

typical LED current reducing to 50% of the minimum value under normal operating condition.

Note (6) Definition of VLED and PLED

$V_{LED} = V_F \times 12$, $I_{LED} = I_F \times 5$, $PLED = V_{LED} \times I_{LED}$



4.5 Power ON/OFF Sequence

1. Interface signals are also shown in the chart. Signals from any system shall be Hi-resistance state or low level when VDD voltage is off.

2. When system first start up, should keep the VDD high time longer than 200ms, otherwise may cause image sticking when VDD drop off.

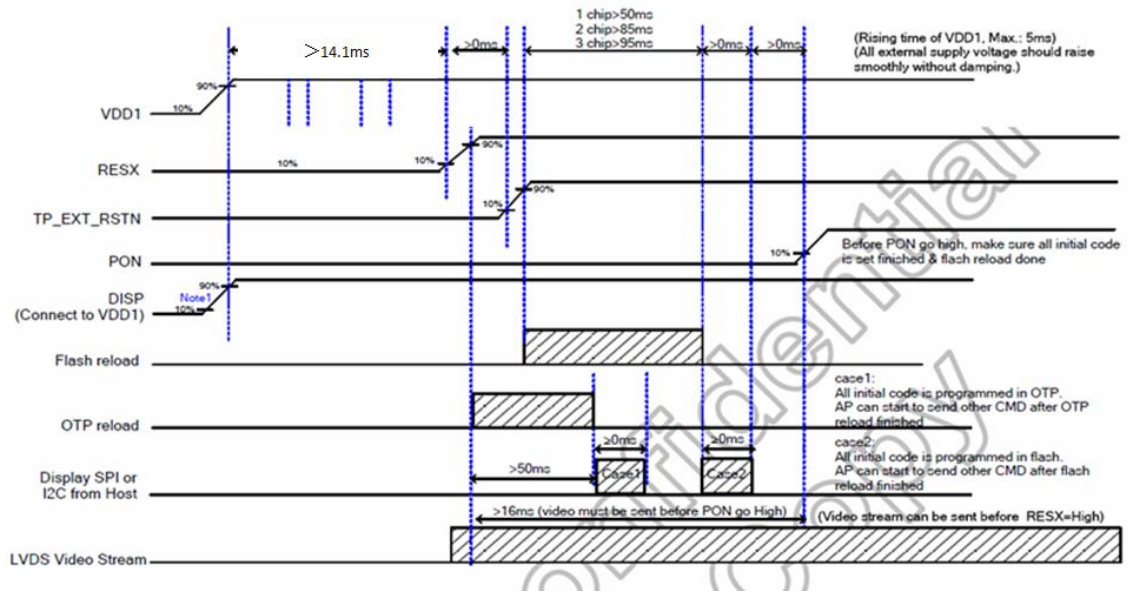


Figure 16 Power on Sequence-1 power mode

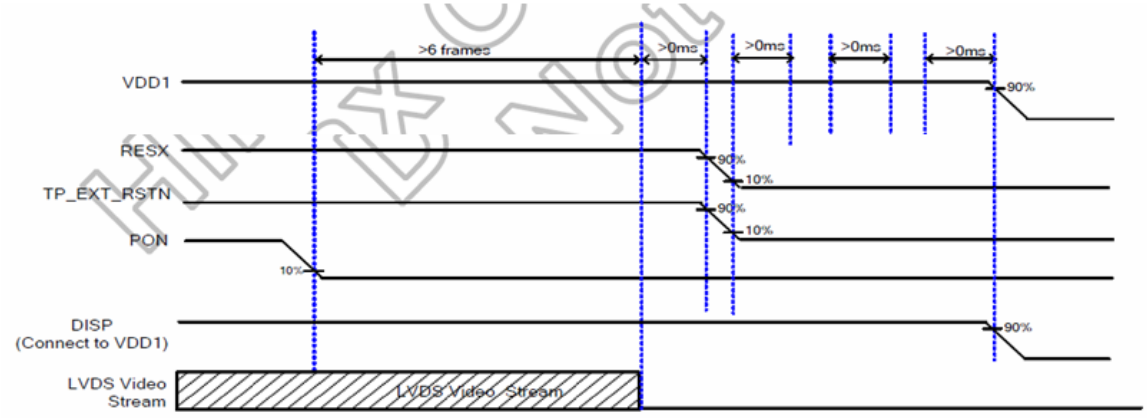


Figure 17 Power off Sequence-1 power mode

5.0 TP Specification

Table 11 TP Characteristics

NO.	Test Item	Test Specification	Copper column diameter
1	Accuracy Test	Center≤1mm,Border≤1.5mm	Φ9mm
2	Jitter Test	Center≤1mm,Border≤1.5mm	Φ9mm
3	Vertical Line Test	Center≤1mm,Border≤1.5mm	Φ9mm
4	Horizontal Line Test	Center≤1mm,Border≤1.5mm	Φ9mm
5	Box Diagonal Line Test	Center≤1mm,Border≤1.5mm	Φ9mm

6.0 Mechanical Characteristics

6.1 Outline Drawing

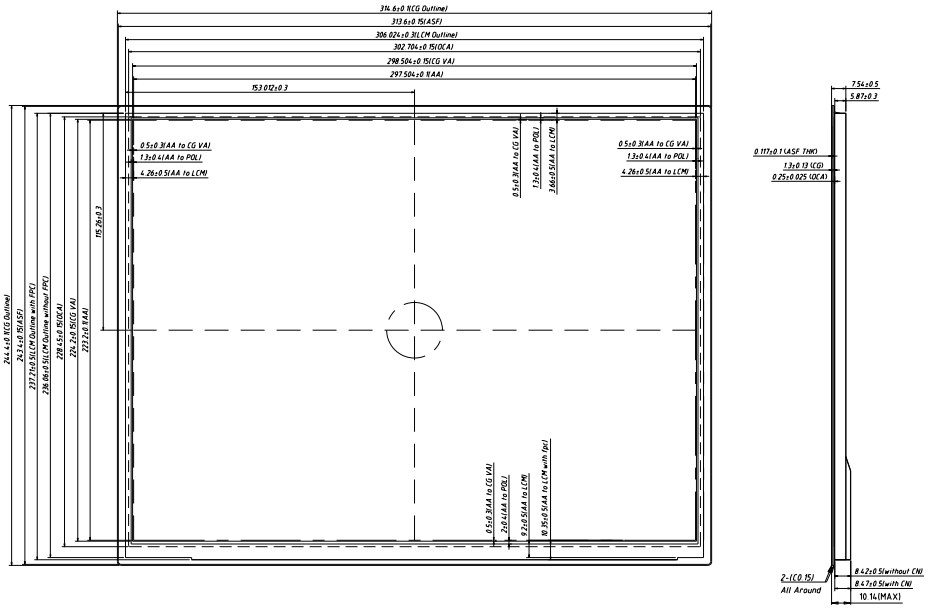


Figure 20 Reference Outline Drawing (Front Side)

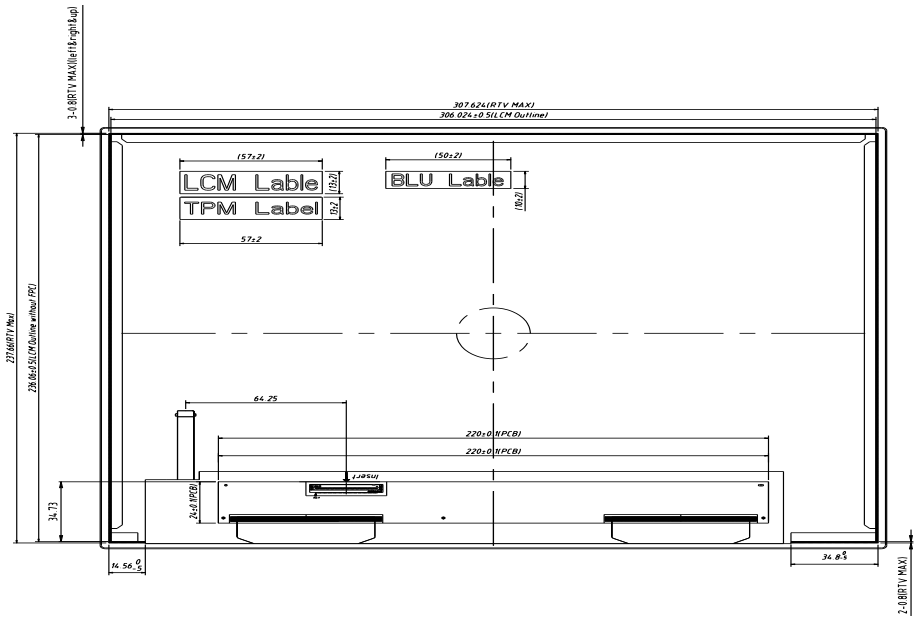


Figure 21 Reference Outline Drawing (Back Side)

Note (1) Unmarked tolerance±0.5mm.

6.2 Dimension Specifications

Table 12 Module Dimension Specifications

Item	Min.	Typ.	Max.	Unit
Width	(314.5)	(314.6)	(314.7)	mm
Height	(244.3)	(244.4)	(244.5)	mm
Thickness	-	-	(10.14)	mm
Weight	-	-	(1,042)	g

Note：Outline dimension measure instrument: Vernier Caliper.

7.0 Reliability Conditions

Table 13 Reliability Condition

Item		Package	Test Conditions	Note
High Temperature/High Humidity Operating Test		CG	T_{gs}=60°C/90% RH,500hrs	(1),(2),(3),(4)
High Temperature Operating Test		CG	T_{gs}=85°C,500hrs	
Low Temperature Operating Test		CG	T_a=-30°C,500hrs	
High Temperature Storage Test		CG	T_a=95°C,500hrs	(1),(3),(4)
Low Temperature Storage Test		CG	T_a=-40°C,500hrs	
Shock Non-operating Test		CG	100G,6ms,sin wave,±XYZ×3times, Total 18times	(1),(3),(5)
Vibration Non-operating Test		CG	half-sine Frequency: 8Hz ~ 33Hz Stroke: 1.3mm Sweep: 2.9G 33.3Hz ~ 400Hz X,Z Cycle : 15 minutes 2 hrs for each direction of X,Z ; 4 hours for Y direction	
Image Sticking	Normal temperature （25℃）	CG	5*7 chessboard Patten, Change to Gray 50% pattern ; Check Point:2hrs(10s)/4hrs(10s)/ 8hrs(2min) 24hrs(5min), ND8% invisible at each check point	(1),(2),(7)
	High temperature (70°C)	CG	5*7 chessboard Pattern, Change to Gray 50% pattern ; Check Point:30min(2s) ,ND10% invisible	

Note (1) A sample can only have one test. Outward appearance, image quality and optical data can only be checked at normal conditions according to the IVO document before reliable test. Only check the function of the module after reliability test.

Note (2) The setting of electrical parameters should follow the typical value before reliability test.

Note (3) During the test, it is unaccepted to have condensate water remains. Besides, protect the module from static electricity.

Note (4) The sample must be released for 24 hours under normal conditions before judging. Furthermore, all the judgment must be made under normal conditions. Normal conditions are defined as follow: Temperature: 25℃, Humidity: 55± 10%RH. T_a= Ambient Temperature, T_{gs}= Glass Surface Temperature.

Note (5) The module should be fixed firmly in order to avoid twisting and bending.

Note (6) It could be regarded as pass, when the module recovers from function fault caused by ESD after resetting.

Note (7) It is recommended to follow the nominal parameter specified by IVO before the Image Sticking test. Besides, V_{com} must be adjusted to optimize display quality.

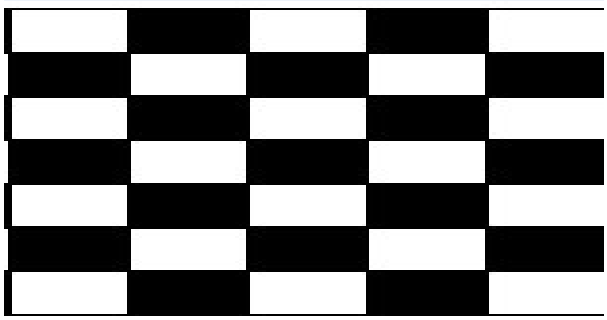


Figure 22 Image Sticking Pattern

8.0 Package Specification

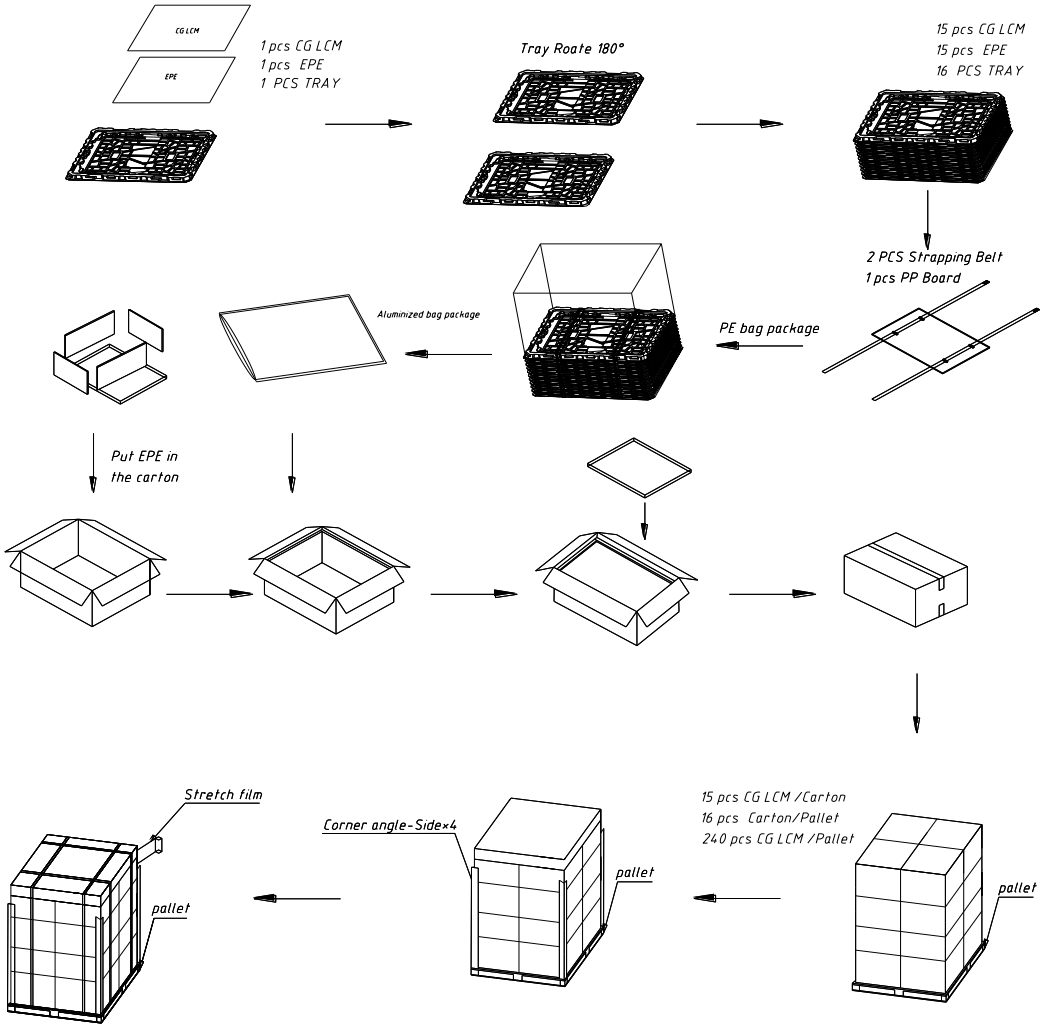


Figure 23 Packing Method

9.0 Lot Mark

TBD

10.0 General Precaution

10.1 Using Restriction

This product is not authorized for using in life supporting systems, aircraft navigation control systems, military systems and any other appliance where performance failure could be life-threatening or lead to be catastrophic.

10.2 Operation Precaution

(1)The LCD product should be operated under normal conditions.
Normal conditions are defined as below:

Temperature: 25℃

Humidity: 55±10%

Display pattern: continually changing pattern (Not stationary)

(2) Brightness and response time depend on the temperature. (It needs more time to reach normal brightness in low temperature.)

(3) It is necessary for you to pay attention to condensation when the ambient temperature drops suddenly. Condensate water would damage the polarizer and electrical contacted parts of the module. Besides, smear or spot will remain after condensate water evaporating.

(4) If the absolute maximum rating value was exceeded, it may damage the module.

(5) Do not adjust the variable resistor located on the module.

(6) Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding may be important to minimize the interference.

(7) Image sticking may occur when the module displayed the same pattern for long time.

(8) Do not connect or disconnect the module in the “power on” condition. Power supply should always be turned on/off by the “power on/off sequence”

(9) Ultra-violet ray filter is necessary for outdoor operation.

10.3 Mounting Precaution

(1) All the operators should be electrically grounded and with Ion-blown equipment turning on when mounting or handling. Dressing finger-stalls out of the gloves is important for keeping the panel clean during the incoming inspection and the process of assembly.

(2) It is unacceptable that the material of cover case contains acetic or chloric. Besides, any other material that could generate corrosive gas or cause circuit break by electro-chemical reaction is not desirable.

(3) The case on which a module is mounted should have sufficient strength so that external force is not transmitted to the module directly.

(4) It is obvious that you should adopt radiation structure to satisfy the temperature specification.

(5) So as to acquire higher luminance, the cable of the power supply should be connected directly with a minimize length.

(6) It should be attached to the system tightly by using all holes for mounting, when the module is assembled. Be careful not to apply uneven force to the module，especially to the PCB on the back.
(7) A transparent protective film needs to be attached to the surface of the module.
(8) Do not press or scratch the polarizer exposed with anything harder than HB pencil lead. In addition, don't touch the pin exposed with bare hands directly.
(9) Clean the polarizer gently with absorbent cotton or soft cloth when it is dirty.
(10) Wipe off saliva or water droplet as soon as possible. Otherwise, it may cause deformation and fading of color.
(11) Clean the panel gently with absorbent cotton or soft cloth when it is dirty. Ethanol(C_2H_5OH) is allowed to be used. Ketone (ex. Acetone), Toluene, Ethyl acid, Methyl chloride, etc are not allowed to be used for cleaning the panel, which might react with the polarizer to cause permanent damage.
(12) Do not disassemble or modify the module. It may damage sensitive parts in the LCD module, and cause scratches or dust remains. IVO does not warrant the module, if you disassemble or modify the module.

10.4 Handling Precaution

(1) Static electricity will generate between the film and polarizer, when the protection film is peeled off. It should be peeled off slowly and carefully by operators who are electrically grounded and with Ion-blown equipment turning on. Besides, it is recommended to peel off the film from the bonding area.
(2) The protection film is attached to the polarizer with a small amount of glue. When the module with protection film attached is stored for a long time, a little glue may remain after peeling.
(3) If the liquid crystal material leaks from the panel, keep it away from the eyes and mouth. In case of contact with hands, legs or clothes, it must be clean with soap thoroughly.

10.5 Storage Precaution

When storing modules as spares for long time, the following precautions must be executed.
(1) Store them in a dark place. Do not expose to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.
(2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.
(3) It is recommended to use it in a short-time period, after it's unpacked. Otherwise, we would not guarantee the quality.

10.6 Others

When disposing LCD module, obey the local environmental regulations.